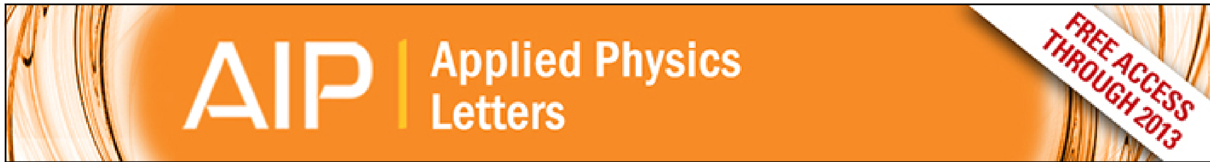

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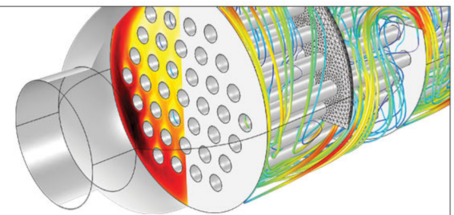

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Boron pileup and clustering in silicon-on-insulator films

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The dopant-defect interaction in silicon-on-insulator (SOI) material is studied for Si film thicknesses ranging from 60 to 274 nm, with regards to (1) boron pileup and (2) defect-induced boron clustering. Results are obtained on boron-implanted samples and on molecular beam epitaxy-grown deposited-boron samples. The experimental results verify simulations predicting (a) boron pileup at both upper and lower interfaces of the Si film, and (b) no reduction of the boron clustering in SOI compared with bulk silicon. © *1999 American Institute of Physics.* [S0003-6951(99)05034-2]

There is great interest in silicon-on-insulator (SOI) technologies because of the possibility of superior low-power behavior and rf response.[1,2] For current complementary metal–oxide–semiconductor (CMOS) technologies with low thermal budget and shallow junctions, accurate process modeling needs to include the interaction between dopants with point defects. In bulk silicon, one of the most important effects of this interaction is the pileup of dopants at the interface of the silicon to gate oxide, induced by excess interstitials.[3] It is caused by the flux of dopant-defect pairs towards the interface which acts as a sink for interstitials, hence, creating a concentration gradient which drives the flux. The effect results in important device behavior, such as the reverse short channel effect (RSCE). Comparing SOI with bulk silicon, the key difference in the physics of the dopant-defect interaction is the addition of the interface between the silicon film and the buried oxide (BOX) layer, referred to as the BOX interface. Crowder *et al.*[4] showed that for partially depleted (PD) SOI devices with the top silicon film thickness (t_{Si}) of 180 nm, the RSCE was reduced compared with devices on bulk Si, indicative of reduced pileup at the front surface, and they ascribed this reduction to the BOX interface acting as an additional sink for interstitials. In this study, the effect of the BOX interface is examined more closely. In future SOI technologies, fully depleted (FD) SOI devices are likely to be employed. In FD devices, unlike PD and bulk devices, the dopant profile under the gate region throughout the *entire* Si film affects the MOS device, hence, the dopant profile at the BOX interface becomes important. We report experimental observations of boron pileup at the BOX interface, and reproduce the results with simulations which assumed that the BOX interface acted as a perfect sink for interstitials. In the second part of this work, we examine whether the BOX interface has an effect on the defect-induced clustering and diffusion of boron at the high concentration necessary for device contact doping.

The SOI wafers in this study were formed by wafer bonding using the SmartCut™ process, with a BOX thickness of 200 nm and t_{Si} of 60 or 70 nm after thinning by oxidation. Subsequent processing steps are detailed in Table I. These may include an additional silicon layer deposited by molecular beam epitaxy (MBE) with a boron spike within the deposited layer.

Secondary ion mass spectroscopy (SIMS) analysis on samples I(a) and I(b), which were doped by boron implantation, clearly shows boron pileup at both Si–SiO_2 interfaces of the SOI film (Fig. 1). Sample I(b) with the additional Si implant shows enhanced diffusion of boron in the film, as expected,[5] as well as a larger amount of pileup boron at both upper and lower interfaces. This indicates that the observed pileup at the interfaces are caused by the additional point defects created by the Si implant. However, because of damage from the boron implant, sample I(a) also shows some pileup. To eliminate the implant damage from boron doping, MBE was used to deposit a boron spike. Figure 2 compares the boron profiles for the as-grown sample, and the processed samples II(a) and II(b). Without additional point defects from the silicon implant, the annealed sample II(a) shows little diffusion compared with the as-grown profile, and more importantly, there is no suggestion of boron pileup at the BOX interface. In contrast, sample II(b) with the silicon implant shows a large diffusion and a pronounced boron pileup at the BOX interface. The clear comparison between samples II(a) and II(b) verifies that we have indeed observed boron pileup at the BOX interface, and that it is due to the presence of excess point defects and not due to artifacts of processing or SIMS analysis. To quantify the enhanced diffusion and pileup effects, process simulation, using the PROPHET tool,[6] is used to model the diffused profile. The simulations assumed a perfect sink for interstitials at the BOX interface. The effective interstitial diffusivity, $D_{i\mathrm{EFF}}$, in the MBE-grown material is set at $1.5\times10^{-12}\,\mathrm{cm}^2\,\mathrm{s}^{-1}$ for 800 °C, the value obtained from similar MBE-grown samples on bulk silicon.[7] This $D_{i\mathrm{EFF}}$ value is greatly reduced from that obtained in metal diffusion experiments[8] since the net motion of interstitials is affected by trapping due to defects in the silicon.[9] For the SOI layer, different values of $D_{i\mathrm{EFF}}$ were tried. In Fig. 3, the curve labeled ''simul 1'' corresponds to a simulation which assumed that both the SOI and

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TABLE I. Processing details.

Sample	t_{Si}	Doping	Si implant	Anneal
I(a,b)	60 nm	10 keV B, 1×10^{13} cm^{-2} +1050 °C, 60 s	I(a) none I(b) 40 keV, 5×10^{13} cm^{-2}	800 °C, 30 min
II(a,b)	70 nm+ 133 nm by MBE	1×10^{18} cm^{-3} spike width=10 nm, by MBE	II(a) none II(b) 25 keV, 1×10^{14} cm^{-2}	800 °C, 30 min
III	70 nm+ 204 nm by MBE	5×10^{19} cm^{-3} spike width=10 nm, by MBE	40 keV, 5×10^{13} cm^{-2}	800 °C for 5 s, 50 s, 500 s

MBE layers have $D_{i\mathrm{EFF}}$ of $1.5\times10^{-12}\,\mathrm{cm^2\,s^{-1}}$. This simulation matches the measured profile in the MBE layer, but overestimates diffusion in SOI, and also does not capture the asymmetry of the SIMS profile. For ''simul 2,'' $D_{i\mathrm{EFF}}$ is set to $1\times10^{-11}\,\mathrm{cm^2\,s^{-1}}$ for SOI, which is typical for the Czochralski material from which the SOI layer was cut. This simulation results in a highly asymmetric profile which underestimates the diffusion in SOI. The best fit (''simul 3'' in Fig. 3) is obtained with SOI $D_{i\mathrm{EFF}}$ of $2.5\times10^{-12}\,\mathrm{cm^2\,s^{-1}}$, indicating that the SOI layer has more interstitial traps than typical Czochralski substrates, but less than MBE-deposited material. In all simulations, the equilibrium interstitial concentration, $C^*_{i\mathrm{TOT}}$ is chosen such that $D_{i\mathrm{EFF}}\times C^*_{i\mathrm{TOT}}$ is constant, as it should be for immobile traps according to Ref. 9 and the product is set to equal that measured by Bracht.[8] $C^*_{i\mathrm{TOT}}$ is the equilibrium value of the total interstitial concentration, $C^*_{i\mathrm{TOT}}=C^*_i+C^*_{i\mathrm{trap}}$, where C^*_i and $C^*_{i\mathrm{trap}}$ are the equilibrium concentrations of the free and trapped interstitials, respectively. The final simulation (''simul 3'') agrees well with both the diffusion and the pileup at the BOX interface. The apparent underestimate of the pileup is due to enhancement in the SIMS signal at the BOX interface: Fig. 1 shows that the boron signal is enhanced by an order of magnitude in oxide compared with bulk silicon. The expected pileup at the surface could not be measured because of surface contamination present in all three cases.

Previous studies in bulk silicon showed that as the thermal budget of processing steps decreased to minimize boron diffusion, less boron is activated than would be expected from equilibrium studies because of the clustering of boron with interstitials.[10,11] The phenomenon is of practical importance because it makes it difficult to attain an ultrashallow *p*-doped junction with low resistivity. Using Monte Carlo simulations with the same model as in Ref. 11, the boron clustering and diffusion in SOI are compared with those in a bulk sample. Figure 4 shows that for an 800 °C anneal, the fraction of boron found in clusters is not different for SOI, and the extent of diffusion of the electrically active boron after 5 and 50 s anneals is also unchanged. After a 500 s anneal, though, there is a small reduction in the diffusion in SOI. This can be understood from the Monte Carlo model:[11] since boron–interstitial clustering occurs early in the implant and anneal processes, when there is a large supersaturation of both interstitials and vacancies, the extra sink for the point defects at the BOX interface makes little difference to clustering. After recombination of the majority of defects (during the ''+1'' regime[12]) the extra sink results in less diffusion in SOI for the 500 s anneal. This predicted behavior is tested experimentally using sample III. Figure 5 shows that the measured results are in excellent agreement with the simulated curves, both for the fraction of boron bound in clusters as well as the extent of diffusion after 5, 50, and 500 s anneals. In addition, the boron pileup at the BOX interface is observed again, in both the measured and simulated data.

We have studied the effect of the BOX interface in SOI materials on two phenomena caused by dopant-defect interactions, by experiments with implanted and MBE-deposited

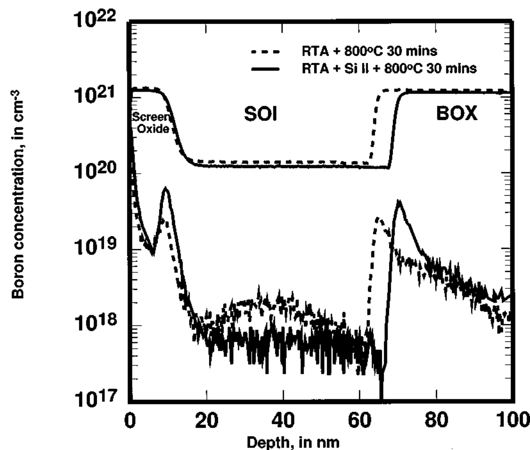

FIG. 1. SIMS measurements of samples I(a) (dashed curve) and I(b) (solid curve). The upper curves show the silicon signals in arbitrary units, and indicate the locations of the interfaces. The lower curves show boron concentrations. SIMS signals were obtained from a CAMECA IMS-6F with a 1 keV O_2^+ primary beam at 60°, giving a penetration depth of only 1.1 nm. The intrawafer variation which resulted from the initial thinning of the SOI from 200 to 60 nm, done prior to the boron implant, caused the 5 nm difference in SOI thickness between samples I(a) and I(b).

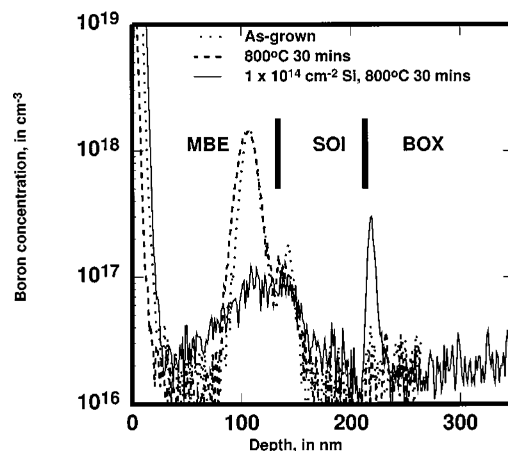

FIG. 2. Boron-doping profiles for the as-grown (dots) and annealed samples II(a) (dashes) and II(b) (thin solid line). Sample II(b) received a 25 keV silicon implant with a dose of $1\times10^{14}\,\mathrm{cm^{-2}}$, and shows both enhanced diffusion and pileup at the BOX interface.

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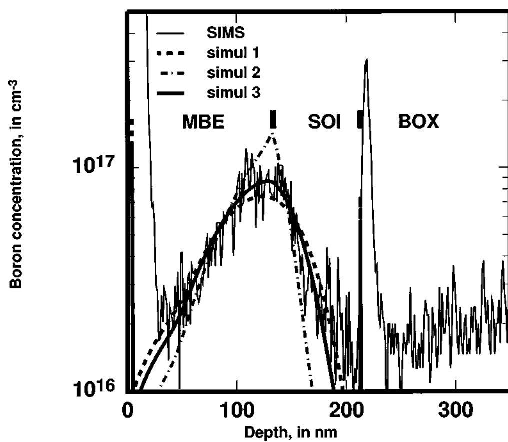

FIG. 3. Comparing the measured diffused profile for sample II(b) with simulated profiles which assumed the effective interstitial diffusivity $D_{i\mathrm{EFF}}$ to be (simul 1) $1.5\times10^{-12}\,\mathrm{cm^2\,s^{-1}}$; (simul 2) $10\times10^{-12}\,\mathrm{cm^2\,s^{-1}}$; and (simul 3) $2.5\times10^{-12}\,\mathrm{cm^2\,s^{-1}}$.

boron-doped wafers, and by process modeling. Our findings are (a) there is a strong pileup effect at the BOX interface whose magnitude is consistent with the assumption of a perfect interstitial sink at the BOX interface, and (b) boron–interstitial clustering, unlike enhanced diffusion, is not affected by the BOX interface. This is consistent with modeling which shows that clustering occurs early in the implant and anneal process.

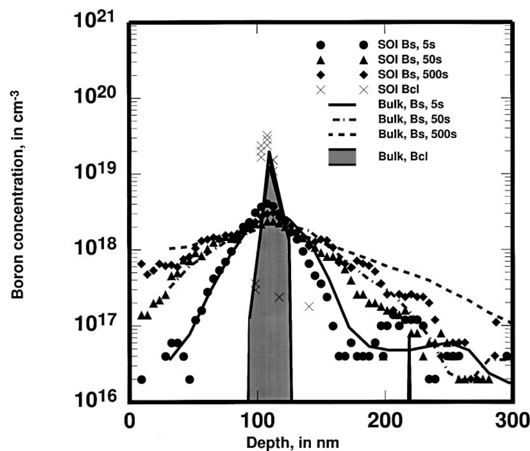

FIG. 4. Simulated profiles of substitutional boron (B_s) and immobile boron–interstitial clusters (B_{cl}) for sample III after 5, 50, and 500 s anneals at 800 °C. There is no change in the B_{cl} profiles during these anneal times, so B_{cl} for all three times collapse to one curve. Symbols represent simulations for a SOI sample with the BOX interface at 280 nm depth, and lines are simulations for a bulk sample.

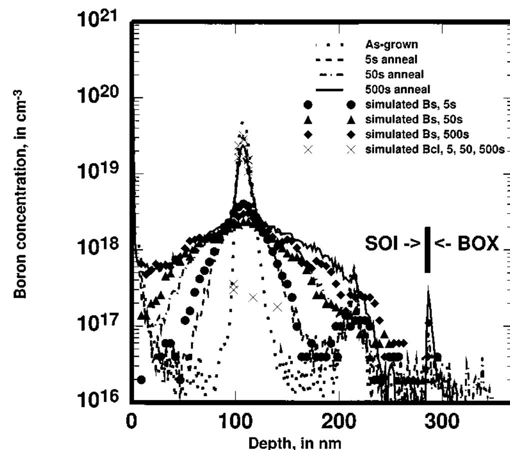

FIG. 5. Lines show the SIMS-measured profiles of sample III as grown (dots), and after annealing at 800 °C for 5 s (dashes), 50 s (stipples), and 500 s (solid). The symbols show the corresponding simulated data, separated into substitutional boron (B_s) and immobile boron clusters (B_{cl}). There is no change in the B_{cl} profiles during these anneal times, so all three times collapse to one set of data.

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