Current Capabilities and Future Prospects of Atomistic Process Simulation

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ABSTRACT

Atomistic process simulators, based on the Kinetic Monte Carlo (KMC) scheme, are an attempt to fulfill some of the ITRS expectations for process modeling and simulation. We present a general overview of its conception and evolution up to its current state, show some of the latest developments, and discuss the possible trends in atomistic process simulation for the coming years.

INTRODUCTION

The requirements of current high-performance MOSFET devices can only be attained through the accurate implementation of complex structures. Their manufacture involves processing steps with many simultaneous physical mechanisms. From the viewpoint of process simulation, both miniaturization and complexity advocate for the use of an atomistic description of the materials and physical mechanisms. Molecular dynamics (MD) would be the most accurate method but it can only simulate very short times, in the range of nanoseconds. KMC was initially used for statistical studies of the annealing of single, isolated cascades [1].

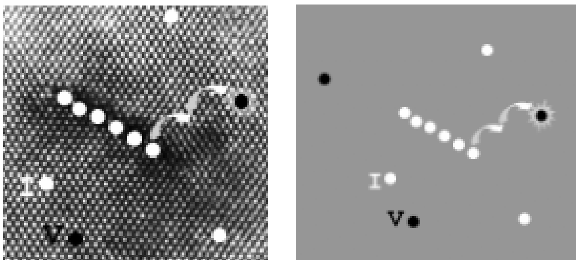

Fig. 1: In contrast to MD, KMC follows only defect atoms (dots in the figure), not the simply vibrating lattice atoms (background).

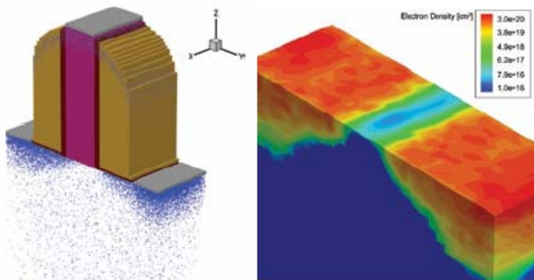

Fig. 2: (From Ref.4). (left) Discrete dopants resulting from a Sentaurus Process KMC simulation and (right) corresponding equilibrium electron concentration. Physical gate length of device is 30 nm.

We have developed an atomistic approach to process simulation (DADOS) based on a KMC diffusion scheme [2]. As a non-lattice KMC, it only follows the defect atoms and impurities (Fig.1). The main advantage is that, instead of using a constant time step like MD (around 10^{-15} s), it performs events (diffusion jumps, emissions, captures…) and calculates the corresponding elapsed time, which can range from 1 ps to several hours. Among other results, it for the first time unveiled the mechanisms leading to the success of empirical the "+1" model for transient enhanced diffusion. After several years of development, essentially all the relevant mechanisms have been incorporated so that it is already included as an option in a commercial 3D TCAD process simulator (Fig.2) [3]. Other research groups have also developed simulators following the same scheme (Fig. 3).

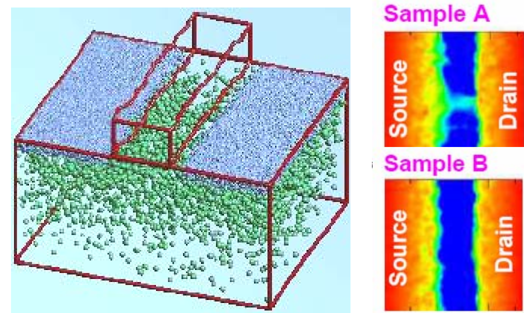

Fig. 3: (From Ref.5). Atomistic KMC process simulation for a MOSFET showing random discrete dopants, one of the sources of intrinsic fluctuations.

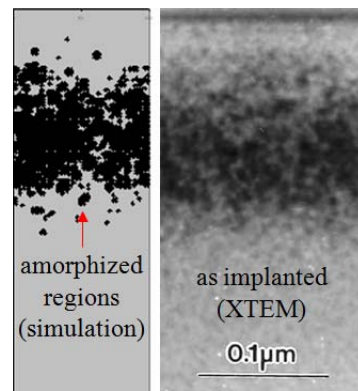

Fig. 4: Simulated damage cross section and experimental XTEM of an implanted silicon wafer [6]. For these nominally non-amorphizing conditions the simulation already predicts small amorphized regions (dark areas) in correspondence with the dark, highly damaged regions observed by TEM.

CURRENT CAPABILITIES

Throughout the development of the current version of our KMC process simulator, a number of publications have addressed different processing conditions and mechanisms. As an example of the degree of realism provided by atomistic KMC, Fig. 4 shows the small amorphized regions from the simulation in correspondence with the "high damage" regions seen in the cross-section TEM picture. This accurate description is not just qualitative but also quantitative as it can be seen in Fig.5 for the amorphous layer thickness. Upon annealing, DADOS provides again a highly realistic view of the recrystallization and damage evolution into clusters and extended defects like voids, {311}'s and dislocation loops (Fig. 6).

Charge effects, that are especially important for dopant diffusion in extrinsic conditions, have been incorporated in the simulator by means of a computationally efficient algorithm that links the discrete point charges with the Fermi-level distribution [8]. Many more mechanisms (recrystallization front with swept/deposited impurities, segregation/trapping at interfaces…) and enhancements have finally allowed the prediction of device characteristics of CMOS devices even for novel co-implants [7]. In particular, atomistic KMC is a natural simulation tool to account for random dopant fluctuation effects (Fig.3), one of the contributions to the variability issues [9] that can preclude the development of the ultimate CMOS

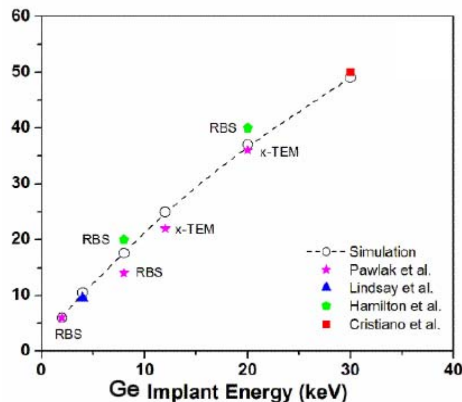

Fig. 5: (From Ref.7) Amorphous layer thickness (nm) as a function of Ge^+ energy at a dose of $1x10^{15}cm^{-2}$.

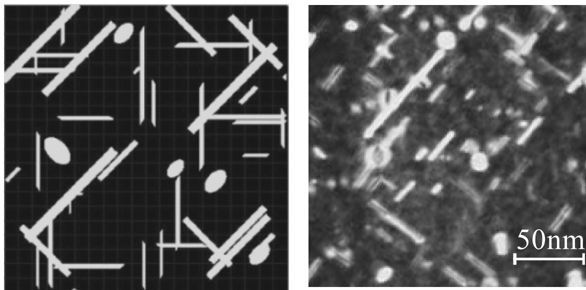

Fig. 6: Plan-view of simulated (left) and experimental (right, from Ref. 6) {311}-defects and dislocation loops after post-implant anneal of the damage shown in Fig. 4.

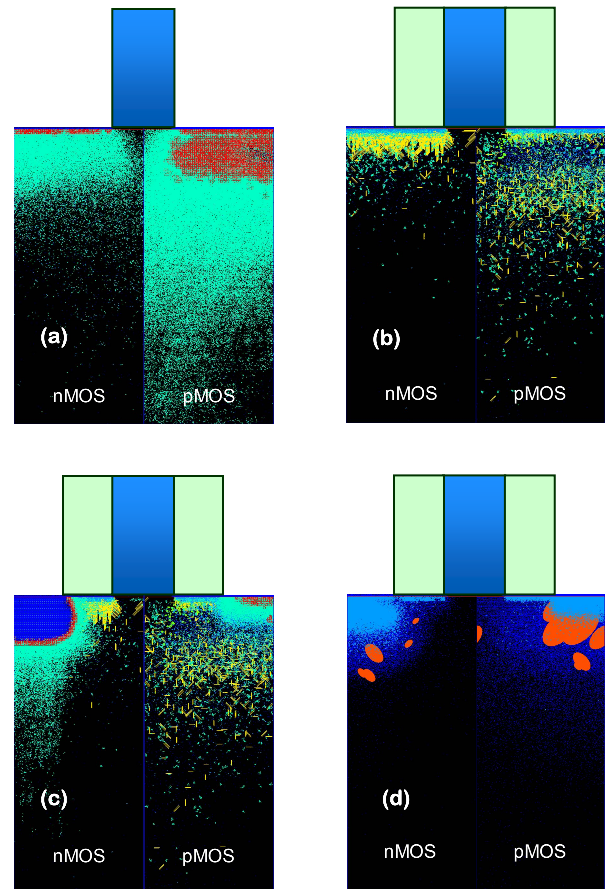

Fig. 7: Typical KMC snapshots from conventional 45-nm planar CMOS processing simulation. (a) Pockets with 30 KeV BF_2 and 50 KeV As and LDD with 1 KeV As and 1 KeV BF_2. (b) Spacers formation anneal. (c) S/D with 15 KeV As and 1 KeV B. (d) Spike [10].

scaling nodes. A typical 45-nm planar CMOS processing sequence is depicted in Fig.7. The small dimensions involved in SOI FET processing make KMC a particularly efficient simulation tool due to the reduced number of defect atom jumps that need to be simulated. Fig.8 shows the good agreement with experimental results of the resultant sheet resistance.

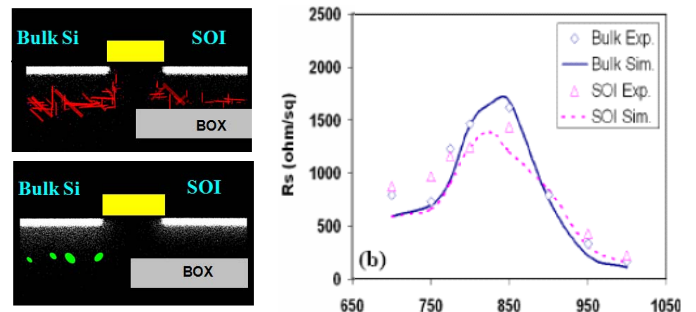

Fig. 8: Sheet resistance as a function of annealing temperature in both bulk Si and SOI. [7]

We have recently developed an atomistic model for stress and SiGe composition effects. Within our approach, the change of dopant diffusivity and segregation has been described through the variation of the formation energy of dopants and defects as well as the charge levels of dopant-defect pairs. It is complemented with a description of the electronic structure (with band splitting) which plays a role in dopant diffusion, especially in extrinsic conditions. Non-hydrostatic, stress-induced anisotropy has been included in the migration rates. Also, an atomistic implementation of Si-Ge interdiffusion has been incorporated. Within this approach, different Si and Ge self-diffusivities are achieved by defining a different probability of an interstitial (I), or a vacancy (V), for moving a Ge or a Si atom. The effects of I (or V) supersaturation on Si-Ge interdiffusion are thus automatically accounted for.

Fig. 9 shows the good agreement with experimental data of Ge self-diffusivities for all Ge compositions. In Fig. 10, B-diffusivity and band-edge profiles are plotted for a uniformly B-doped $Si/Si_{0.7}Ge_{0.3}$ abrupt structure at the beginning of a 900ºC anneal. Extrinsic B diffusivity is controlled by the distance of the B-I pair charge level to the Fermi-level. Fig. 11 depicts the resulting segregation of B upon diffusion from Si to strained SiGe layers. Fig.12 is a 2D plot of a 3D atomistic simulation, showing the effect of stress on As diffusion in a 32-nm node strained silicon FET as well as the intrinsic dopant fluctuations.

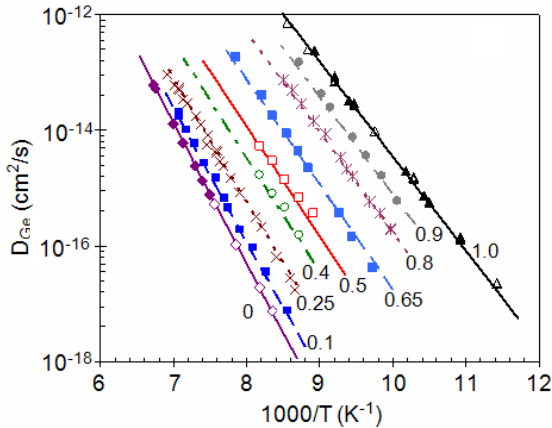

Fig. 9: Ge self-diffusivity in $Si_{1-x}Ge_x$. Symbols: experimental data [11-13]. Lines: model.

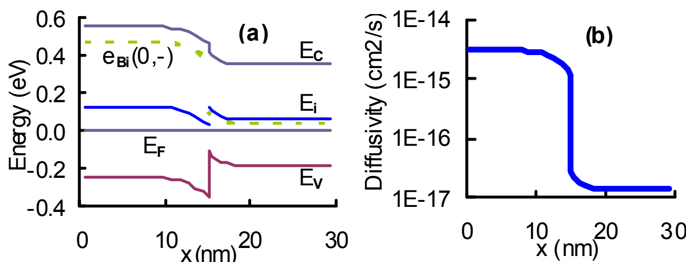

Fig. 10: (a) Band-edges and (b) extrinsic B-diffusivity profile for a 10^{19} cm^{-3} B-doped $Si/Si_{0.7}Ge_{0.3}$ abrupt structure, lattice matched to Si, at 900ºC.

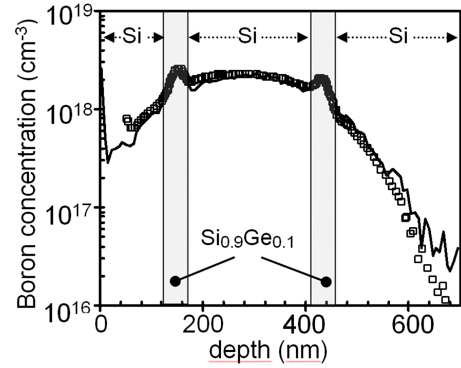

Fig. 11: Annealed experimental and simulated B concentration profiles in Si/SiGe strained structures [14].

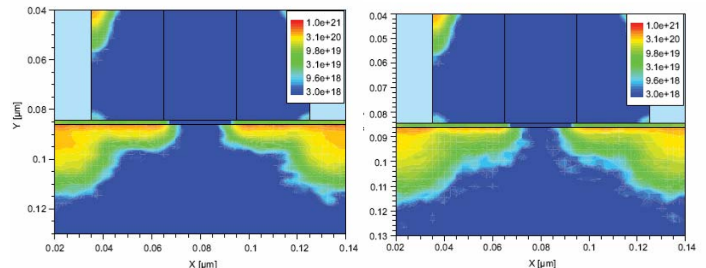

Fig. 12: (From Ref. 4) Simulated concentration of active arsenic under spacer and gate of a 32 nm node technology FET device in (left) relaxed and (right) strained silicon performed with Sentaurus Process KMC .

Regarding the current trend to switch from a batch implanter to a single wafer, effective dose rate can play a significant role [15] but dose rate is not accounted for in continuum simulators. KMC process simulations, which include dose rate and target temperature effects, reveal that indeed the amorphous layer thickness are expected to be slightly different (Fig.13).

Atomistic KMC is advantageous the smaller the device volume. As an example, the complete damage anneal of the S/D deep-implant plus extension of a 20 nm-NMOSFET [17], using a simulation cell of 100×70×50 nm^3, takes only 10 min on a 2GHz PC. Notice that in KMC usually all models are active simultaneously since the computation time only increases slightly by the incorporation of new mechanisms.

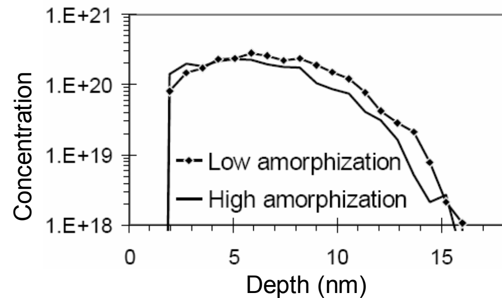

Fig. 13: Simulated profiles of clustered B at R_p after anneal, for a single wafer implanter (low amorphization) and for a batch implanter (high amorphization). Although the dose rate is nominally the same for both, the amorphized thickness is slightly different due to the different implant pulses [16].

PROSPECTS

According to the analysis of alternative technologies carried out by the ITRS, none of them is clearly superior to MOSFETs for performing Boolean logic operations. The most likely scenario for high-performance as well as for low-power logic is, therefore, the continued use of the MOSFET structure (Planar, FD-SOI, Multi-Gate…) up to nearly its physical limits. For the next decade or so, as the device size continues to shrink to its limit, atomistic KMC can be expected to settle as a mature and advantageous process simulation framework to complement [7] or extend the continuum approach. However, the upcoming non-planar MOS devices (UTB FD, Fin-FET, Multi-Gate) use extremely thin layers built through growth, etch and deposition, which are still missing (with atomistic implementation) in non-lattice KMC. But these processes, together with the absence of implant damage and the dominant role of interfaces and grain boundaries, prompts to Lattice KMC (L-KMC) as a favorite candidate. For instance, L-KMC is able to generate the variety of morphologies that can arise during deposition, depending on the particular processing conditions (temperature, deposition rate, substrate conditions, etc.), from the very beginning of the nucleation processes (figs.14,15) up to the simulation of polycrystalline thin films (fig.16). These and other features would make L-KMC especially apt for the simulation of ultimate scaled MOS devices.

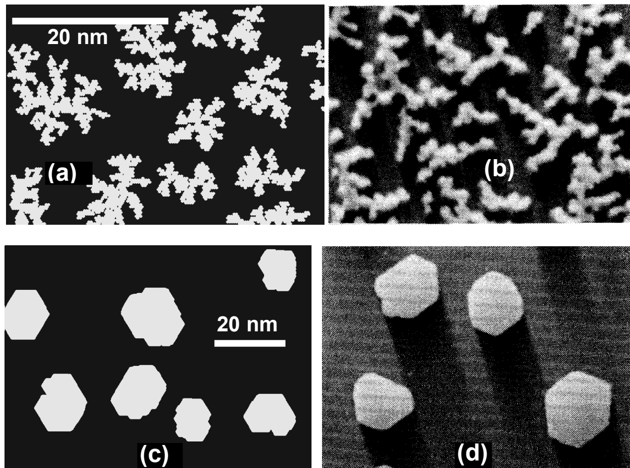

Fig. 14: Grain nucleation on FCC (111) oriented. (a) and (b): Al onto Al simulations at 120K and 450K; (c) and (d): Pt onto Pt STM measurements at 200K and 455 K [19].

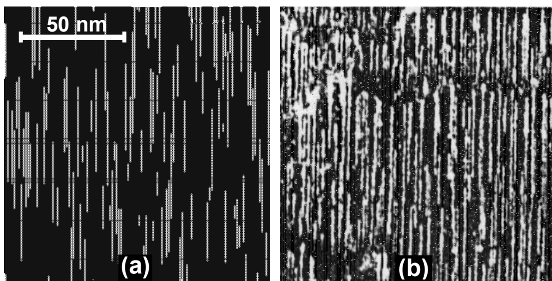

Fig. 15: Grain nucleation on FCC (110) oriented. (a): Al onto Al simulations at 300K; (b) Cu onto Pd STM measurements at 265K [20].

CONCLUSIONS

The most genuine strength of KMC is that it can handle many mechanisms simultaneously, as needed in complex device processing. In addition, these mechanisms are directly linked to microscopic physical parameters, which can be obtained from ab-initio calculations or experimental measurements. As a result, it can be highly predictive. It is not meant to compete in accuracy with ad-hoc simulation approaches, calibrated for specific conditions. The goal, instead, is to attain a simulator that, although not extremely accurate for any particular conditions, never gives a totally wrong result, even for previously unexplored processing parameter ranges. In conclusion, KMC can be a helpful simulation tool to assist process engineering groups find acceptable parameters windows for the complex processing involved in ultimate CMOS scaling technologies.

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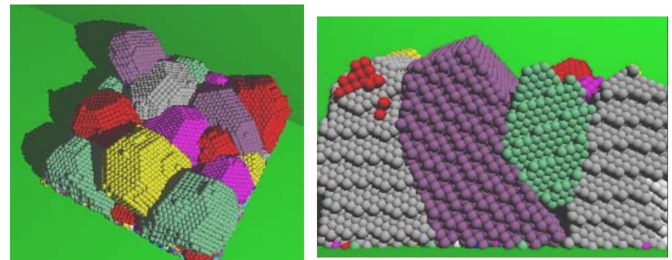

Fig. 16: Lattice-KMC can simulate polycrystal phenomena like faceting, grain growth, and grain boundary diffusion [21]. Left: 3D view. Right: cross-section.