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Modeling and Simulation of the Influence of SOI Structure on Damage Evolution and Ultra-Shallow Junction Formed by Ge Preamorphization Implants and Solid Phase Epitaxial Regrowth

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ABSTRACT

Preamorphization implant (PAI) prior to dopant implantation, followed by solid phase epitaxial regrowth (SPER) is of great interest due to its ability to form highly-activated ultra-shallow junctions. Coupled with growing interest in the use of silicon-on-insulator (SOI) wafers, modeling and simulating the influence of SOI structure on damage evolution and ultra-shallow junction formation is required. In this work, we use a kinetic Monte Carlo (kMC) simulator to model the different mechanisms involved in the process of ultra-shallow junction formation, including amorphization, recrystallization, defect interaction and evolution, as well as dopant-defect interaction in both bulk silicon and SOI. Simulation results of dopant concentration profiles and dopant activation are in good agreement with experimental data and can provide important insight for optimizing the process in bulk silicon and SOI.

INTRODUCTION

Ultra-shallow junction formation by solid phase epitaxial regrowth (SPER) has been shown to be capable of achieving junction characteristics (depth, abruptness, sheet resistance values) that meet the transistor requirements for the 45 nm CMOS node [1]. The technique for the formation of ultra-shallow junctions with boron consists of preamorphizing the substrate prior to dopant implantation, followed by a low temperature SPER process. The amorphous silicon reduces dopant channeling, resulting in abrupt, shallow profiles, while SPER at low temperature, allows only slight diffusion and incorporates dopant atoms into substitutional lattice sites at metastably high concentrations above the equilibrium solid solubility limit [2]. This is an attractive technique as it requires only conventional implant and thermal processing equipment.

The use of silicon-on-insulator (SOI) in place of conventional bulk silicon wafers is increasingly popular. SOI offers improved performance and reduced power consumption. Differences in B electrical activation and damage evolution [3] could be expected in the presence of a buried oxide layer, as in the case of SOI, due to the role of oxide interfaces as point defect sinks and the direct correlation between B deactivation and interstitial defect dissolution from the EOR defects [4-7].

It is therefore important to understand and have reliable predictive models to simulate the SPER process and dopant electrical activity in preamorphized silicon in both bulk silicon and

SOI. To achieve this, it is necessary to have a good model for amorphization and recrystallization [8], which will be needed to provide reliable information on the number of interstitials in the EOR region in amorphizing conditions. In addition, it is important to correctly model the transition of extended defects in the EOR, from {311}s to dislocation loops [9]. Due to the difference in interstitial supersaturation of these extended defects, and the fact that B deactivation is driven by the interstitials released from the EOR, it is crucial to correctly predict whether or not, and when, the dislocation loops appear, as this will affect the simulation of dopant electrical activation, as well as the dopant concentration profile.

In this work, we simulate the process for the formation of an ultra-shallow junction by SPER, showing the evolution of the implantation-induced damage, the deactivation and reactivation of boron during isochronal thermal anneals at various temperatures after SPER. In addition, we show the influence of the presence of a buried oxide, as in the case of SOI wafers.

MODEL

Atomistic simulations were carried out using a non-lattice kinetic Monte Carlo (kMC) simulator, DADOS [10] that takes into account amorphization and recrystallization, comprehensive defect interaction and evolution, as well as dopant-defect interaction. The coordinates of the ion-implantation induced point defects were obtained from a binary collision program [11] and inserted into the kMC simulator. In the region where the defects accumulate up to the amorphization threshold, a fully amorphous layer is formed, which upon subsequent thermal anneals, recrystallizes, depositing dopant as active up to a concentration of $2x10^{20}$ cm^{-3} [4]. The remaining B forms small, immobile electrically inactive clusters, B_3I [7, 12]. In the non-amorphized region, interstitials and vacancies recombine, leaving a band of excess interstitials just below the amorphous-crystalline interface. With increasing annealing temperatures, these defects evolve from small interstitial clusters to {311} defects and into dislocation loops. At the same time, the interstitial point defects released from these extended defects at the EOR may diffuse to the B-rich surface to form boron interstitial clusters, thereby deactivating the B. Otherwise, they may be lost to sinks, such as the surface or the oxide interface.

In the simulations shown in this work, the oxide interface was modeled as a perfect sink for the interstitial point defects. SOI wafers were simulated by changing the material from silicon to oxide at depths more than 55 nm, following the structure of the experimental SOI wafers, essentially creating an oxide interface at 55 nm.

SIMULATION RESULTS AND DISCUSSION

In the simulations, bulk silicon and SOI samples were preamorphized by Ge implanted at 8 or 20 keV at a dose of $1x10^{15}$ cm^{-2}, followed by 500 eV B at a dose of $2x10^{15}$ cm^{-2}. This was followed by an isochronal (60 s) anneal in the temperature range of 700 to 1000 ^{o}C. We first show simulation results that are in good agreement with experimental observations of the damage evolution during this process, which gives validity to the subsequent results on dopant concentration profile and dopant electrical activation.

Figure 1 shows the as-implanted damage (interstitial) concentration profile following an 8 or 20 keV Ge implant and a 500 eV B implant. The amorphous depths are close to the 20 and 40

nm respectively determined experimentally by Rutherford Backscattering Spectrometry [5]. Evolution of the EOR defects in the case of the 20 keV Ge preamorphization implant (PAI) is shown in figure 2. After 60 s anneal at 700 ^{o}C, the EOR damage is in the form of small interstitial clusters and {311} defects. At 800 ^{o}C, the EOR damage consists of {311} defects and some dislocation loops. This is consistent with transmission electron microscopy analysis of similar experimental condition (with 30 keV Ge PAI instead) [13]. As mentioned, it is important to correctly predict the damage evolution as it would affect dopant concentration profile and dopant electrical activation.

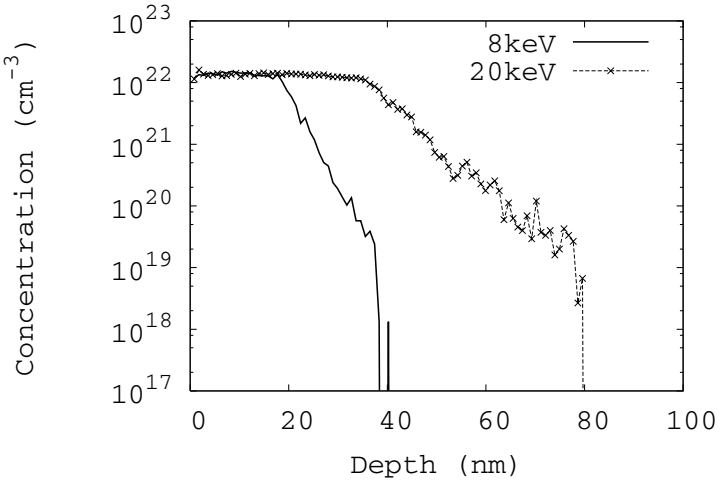
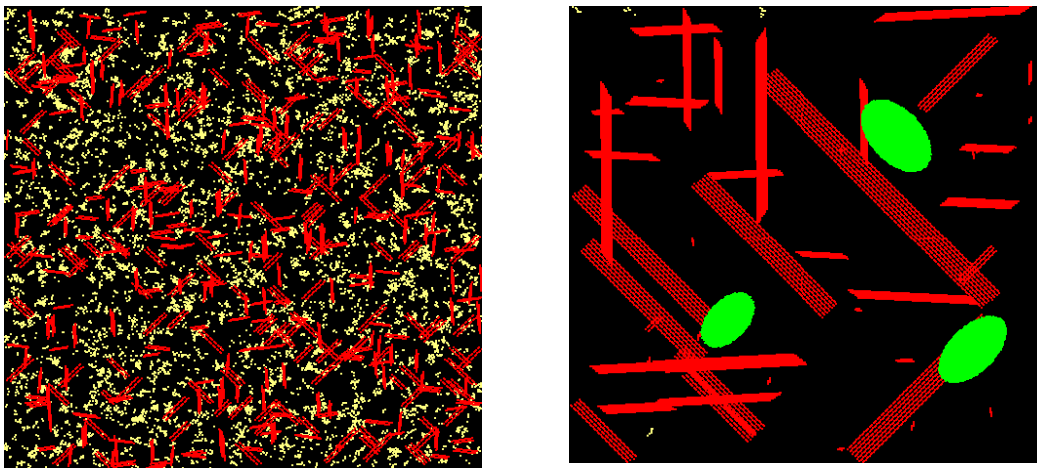


Figure 1. Simulated damage (interstitial) concentration profile of as-implanted 8 and 20 keV Ge, followed by 500 eV B. The saturated (~1x10^{22}cm^{-3}) level corresponds to amorphized material.



(a) **(b)**

Figure 2. Simulated plan-view of defects corresponding to 60 s anneal at (a) 700 ^{o}C (b) 800 ^{o}C of damage induced by 20 keV Ge preamorphization implant at a dose of 1x10^{15} cm^{-2}, followed by 500 eV B at a dose of 2x10^{15} cm^{-2}. Scale: 80nm x 80 nm.

Figure 3 shows the B concentration profiles for the 20 keV Ge PAI case after a 60 s, 850 ^{o}C anneal in bulk silicon and SOI. The simulated B profiles are able to reproduce very well the "kink" in the experimental B profiles [5]. The impact of a buried oxide layer in the SOI case can be clearly seen. Experimentally, the secondary ion mass spectrometry (SIMS) for the B profile in the bulk silicon case (figure 3a) shows a peak in the tail of the boron profile, corresponding to the position of the EOR defect region. This implies that EOR defects and some trapped boron are present in this region in the bulk silicon sample. However, this peak is not seen in the corresponding SOI sample (figure 3b). This implies that EOR defects have been completely annealed out in the SOI case by the same thermal budget. Despite including in the simulator boron pile-up due to dislocation loops [14], the small peak in the B profile (figure 3a) is not observed in the simulated concentration profile in the bulk silicon case. However, interstitial damage (dislocation loops) remains in the same location. In the corresponding case of the SOI sample, no defect is present in the EOR region from the simulation, in agreement with experimental SIMS profile. In all cases, for the same anneal temperature, less defects remain in the EOR in the SOI case than in the bulk silicon case. This can be explained by the presence of the buried oxide layer, providing an additional mode for the removal of the EOR defects.

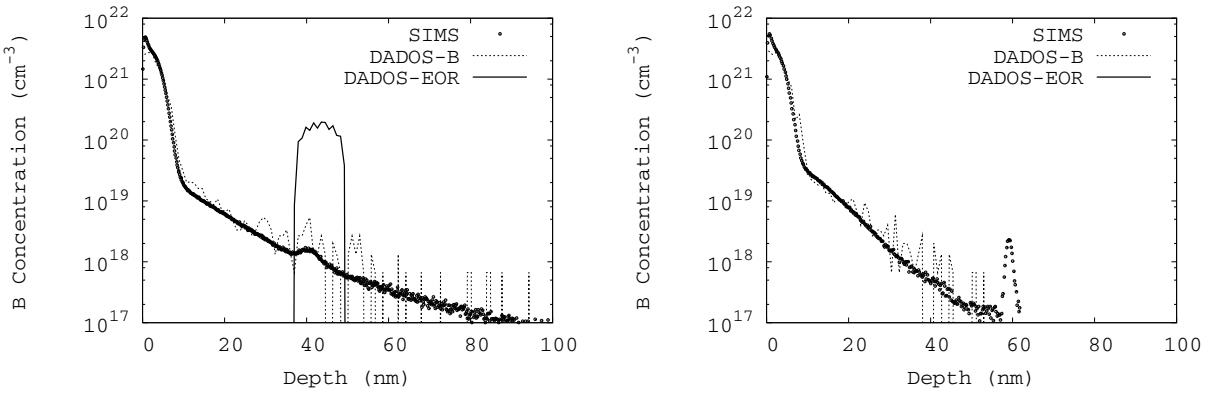


Figure 3. B concentration profile for 20 keV Ge PAI samples after 60 s, 850 ^{o}C anneal in (a) Bulk Si (b) SOI. SIMS obtained from Ref. [5].

A detailed understanding of the process can be obtained from the simulations of the dopant concentration profile, the type and amount of damage remaining and the level of dopant activation. Dopant activation is given by the sheet resistance, which is calculated by

$$R_s = \frac{1}{q\int_0^{x_j} \mu(x) C_B(x) dx}$$

where x_j is the junction depth, $C_B(x)$ the carrier concentration, $\mu(x)$ the concentration dependent hole mobility [15], and q the electronic charge.

Figure 4 shows the variation in sheet resistance as a function of annealing temperature. For both the 8 keV and 20 keV Ge PAI, dopant deactivation is observed as sheet resistance increases

with annealing temperature, up to a maximum, before dopant reactivation occurs, with sheet resistance rapidly decreasing to very low values.

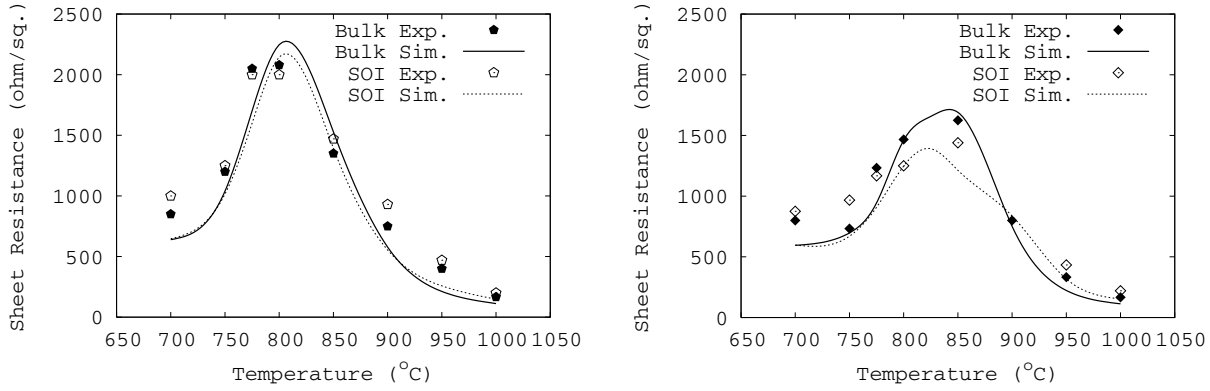


Figure 4. Sheet resistance as a function of annealing temperature, after 60 s isochronal anneal. (a) 8 keV Ge PAI (b) 20 keV Ge PAI. Experimental points from Ref. [5].

The initial rise in sheet resistance (dopant deactivation) occurs during the ripening of EOR defects. The release of the free interstitial point defects from the EOR, diffuse towards the B-rich surface, forming boron interstitial clusters, deactivating B in the process. The subsequent decrease in sheet resistance (dopant reactivation) is mainly related to the dissolution of the boron interstitial clusters.

In the 20 keV Ge PAI case, in agreement with experimental results, the maximum sheet resistance in the SOI case is lower than the corresponding bulk Si case, implying that B deactivates less in SOI. The higher electrical activation in the SOI case is possibly due to the lower amount of interstitials in the SOI sample compared to the bulk Si sample, as shown in figure 3. The overestimation in the difference between the simulated sheet resistance for the bulk Si and SOI case (Fig. 4(b), 850^{o}C) could be the result of assuming the oxide interface as a perfect sink, which may in fact be a partial sink for interstitial point defects.

It is difficult to conclude from the sheet resistance results and the SIMS if the reduced amount of defects in SOI wafer is due to the buried oxide layer acting as a sink for the free interstitial point defects or if there is intrinsically less interstitial defects to begin with in the SOI wafer, as a portion of the as-implanted damage induced by 20 keV Ge PAI case is trapped in the buried oxide (at 55 nm), as can be seen in the simulated profile in figure 1. The latter reason could be likely in light of the experimental Hall sheet resistance results for 8 keV Ge PAI, which shows little difference between the bulk silicon and SOI samples. Alternatively, the little difference in the sheet resistance in the 8 keV Ge PAI case could be due to the fact that the oxide layer is far from the EOR defects that the "sink" effect of the oxide surface is not significant.

To get a better understanding, a test simulation was done using the 20 keV Ge PAI condition, with the buried oxide layer at 80 nm, instead of 55 nm. As one can see from figure 1, placing the oxide interface at 80 nm would not remove the as-implanted damage initially and at the same time, would act as a "sink" close enough to the EOR defects. Based on simulation of 20 keV Ge PAI condition, followed by a 60 s, 850 ^{o}C anneal (corresponding to the condition of figure 3), the EOR damage was also completely annealed out (not shown), implying that the buried oxide

interface acting as an interstitial sink, could affect damage evolution and the remaining EOR. Furthermore, values of sheet resistance in this case are intermediate between the bulk Si case and the case where the buried oxide layer is at 55 nm (not shown).

CONCLUSION

Dopant concentration profile, activation and reactivation have been simulated in both bulk silicon and SOI, in an ultra-shallow junction formation process by the Ge PAI and SPER technique. We show that less defects remain in the EOR in the SOI case compared to the bulk Si case, which leads to less dopant deactivation in SOI. It is found that the position of the oxide interface affects damage remaining in the EOR and dopant activation, as it acts not only as a sink for the EOR defects, but also trapping part of the as-implanted damage.

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