

Design and Optimization of nanoCMOS devices using predictive atomistic physics-based process modeling

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Abstract

For the first time, this work shows that the design and optimization of nanoCMOS devices can be achieved from atomistic physics-based process modeling. Remarkable prediction of device characteristics can be obtained even for novel co-implant processes. This extends the strength of TCAD in manufacturing for future generations of nanoCMOS devices.

Introduction

Kinetic Monte Carlo (kMC) process simulator has long been considered as the future for TCAD as it embeds all the complex atomistic mechanisms involved during the implantation and diffusion steps of the fabrication process (1). Up to now, kMC has only been successfully demonstrated to simulate 1D dopant profiles, especially for boron and arsenic (2-7). However, it has not been applied systematically to get the accurate 2D/3D dopant profiles that can be directly transferred to device simulator. In this work, we demonstrate that kMC DADOS not only can generate accurate 2D/3D profiles for present and future nanoCMOS devices, but can also obtain remarkable prediction of device characteristics for a comprehensive series of novel co-implant processes. This paves the way for the use of kMC in the design of devices and the optimization of device performance in TCAD for manufacturing.

Methodology and predictive simulations

Fig. 1 presents the methodology used to generate accurate 2D/3D dopant profiles for nanoCMOS device simulations. KMC DADOS is capable of simulating the different mechanisms involved during implantation and annealing processes due to the precise description of the dopant, defect diffusion and dopant-defect interaction during annealing. Accurate damage evolution (implanted damage, EOR defects) in agreement with Transmission Electron Microscopy (TEM) is shown in Fig. 2.

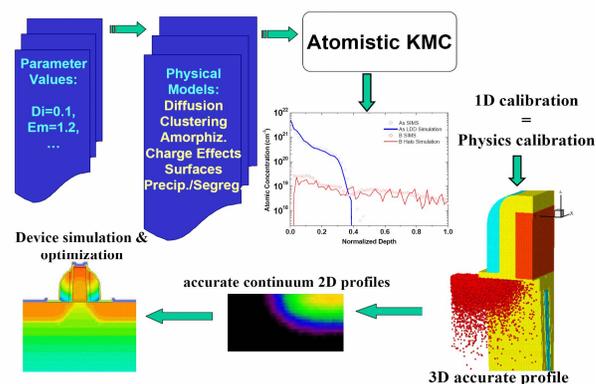


FIGURE 1. Schematic representation of the methodology used to generate accurate 2D/3D profiles for device simulation using kMC simulator.

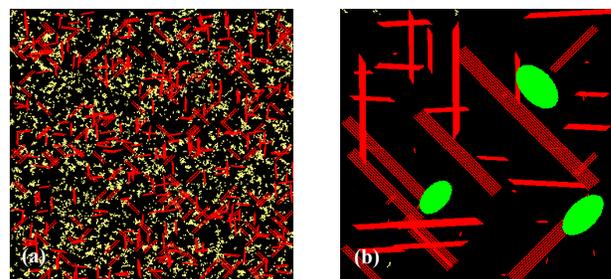


FIGURE 2. Simulated plan-view of defects corresponding to 60s anneal at (a) 700°C (b) 800°C of damage induced by 20 keV Ge preamorphization implant to a dose of $1 \times 10^{15} \text{ cm}^{-2}$, followed by 500 eV B to a dose of $2 \times 10^{15} \text{ cm}^{-2}$. Scale: 80 nm x 80 nm.

In general, a wide range of SIMS, sheet resistance measurements, TEM analyses from dedicated experiments at low temperatures (spacer anneals), spike anneals as well as isochronal and isothermal studies have been used to extract dopant physical parameters. Simulations versus experimental data (7) of Ge pre-amorphized (PAI) boron USJ formation in bulk Si and SOI are shown in Figs. 3-4. The interaction between point defects, extended defects and boron, as well as the role of buried Si/Oxide interface in SOI case are well-reproduced.

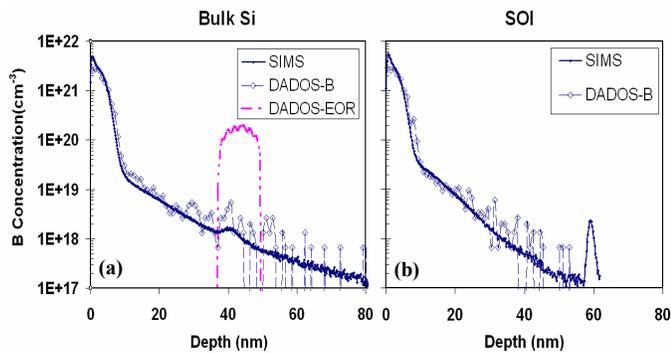


FIGURE 3. Boron concentration profiles for 20 keV Ge PAI samples after 60s, 850 °C anneal in (a) Bulk Si (b) SOI.

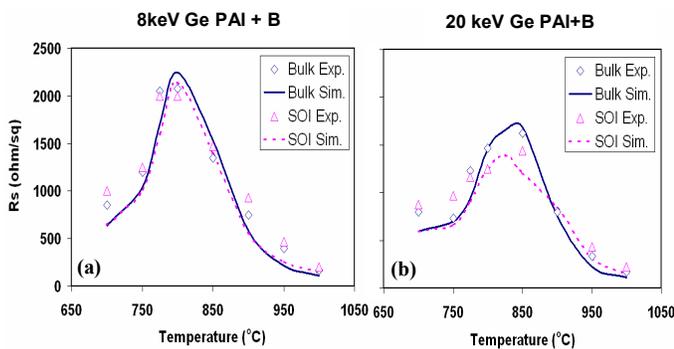


FIGURE 4. Sheet resistance as a function of annealing temperature after 60s isochronal anneal. (a) 8 keV Ge PAI + B (b) 20 keV Ge PAI + B.

For n-type dopant, Arsenic diffusion and clustering are already well-established in the literature (6). However, this is not the case for phosphorus. In agreement with the latest available studies (8-9), we assumed that phosphorus diffuses via interstitial and vacancy pairs, whilst clustering is due to phosphorus-vacancy clusters formation. Our Phosphorus physical parameters are in excellent agreement with intrinsic and extrinsic Phosphorus diffusion, as well as diffusion and activation during spacer and spike anneals (see Figs. 5-6).

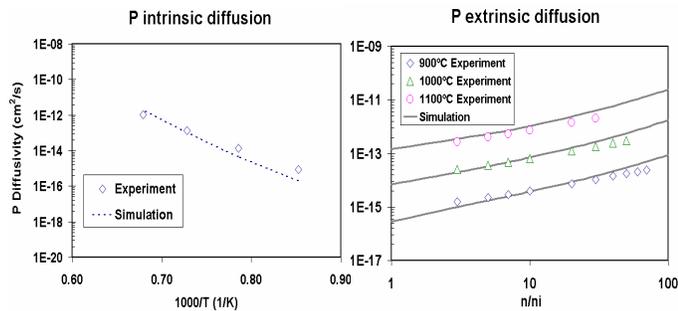


FIGURE 5. Phosphorus intrinsic and extrinsic diffusivities. Symbols are experimental data from literature (9), lines are from simulations.

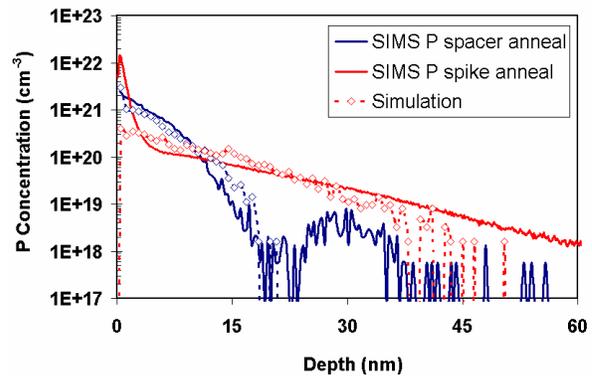


FIGURE 6. Phosphorus concentration profiles for 15keV Ge PAI samples after spacer and spike anneals. Lines are experimental data from literature, symbols are from DADOS simulations.

Based on these accurate physical parameters, we simulated the 2D/3D dopant profiles for 65nm CMOS technology node. Example for 65nm low-power PMOS is shown in Figs. 7-8. Upon transfer to device simulator, excellent prediction of Id-Vg curve as well as Vtsat roll-off is obtained. It should be noted that accurate results are also obtained for predictive simulations of mature technologies such as 0.13um or 0.18um (10).

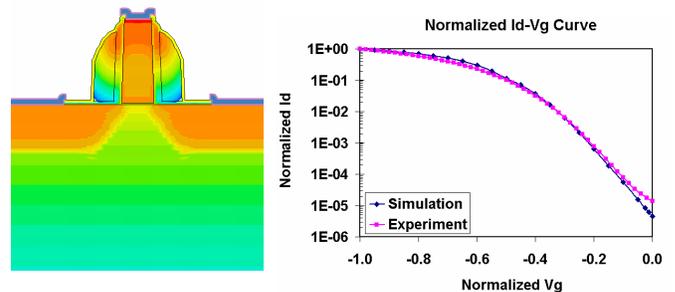


FIGURE 7. 2D simulated profiles for 65nm PMOS and Id-Vg comparison with benched data.

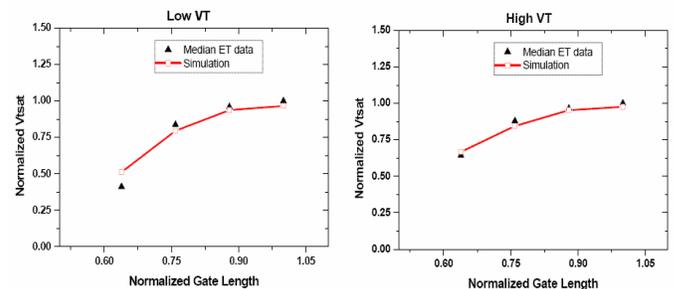


FIGURE 8. Comparison between experimental and simulated PMOS roll-off behavior.

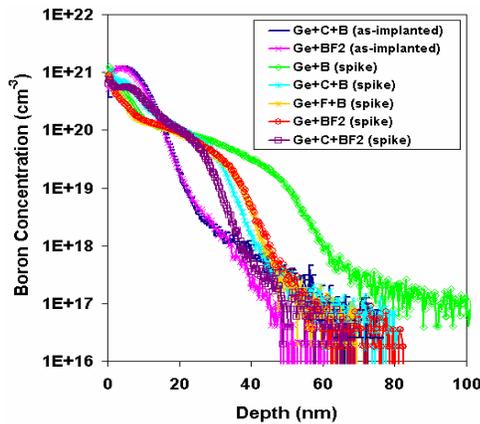


FIGURE 9. SIMS profiles showing the impact of different co-implant conditions on PMOS junction formation. Best junction obtained for BF₂ co-implanted with Carbon.

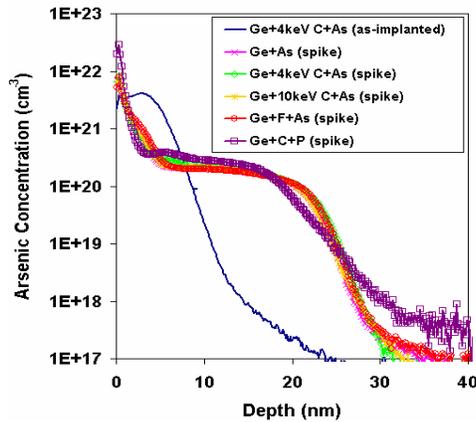


FIGURE 10. SIMS profiles showing the impact of different co-implant conditions on NMOS junction formation. Carbon co-implantation allows the formation of highly-activated junction for the Phosphorus case.

Applications: novel co-implant processes and 3D SRAM

As technology moves forward, new alternatives have to be considered to improve junction and device performances. Among them, co-implants with impurities are of great interest (11-14). However, difficulties arise from a lack of prediction of these novel alternatives, which obstructs the device design and process optimization. Figs. 9-10 show the drastic co-implant effect on P+/N and N+/P junction characteristics. To predict such behaviors, we first extracted Carbon and Fluorine diffusion and clustering parameters from literature (14-17). For Carbon, carbon-interstitial clustering has been taken into account, whilst for the Fluorine case, clustering with vacancies is considered.

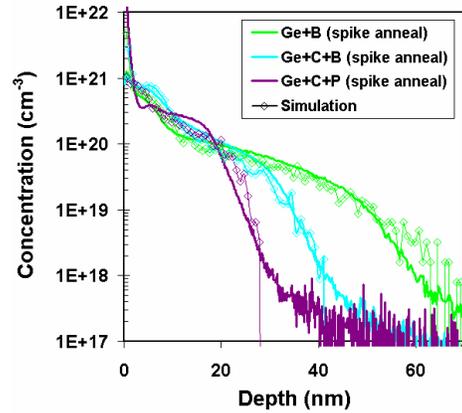


FIGURE 11. Comparison between simulated and experimental profiles of Carbon co-implants on dopant diffusion.

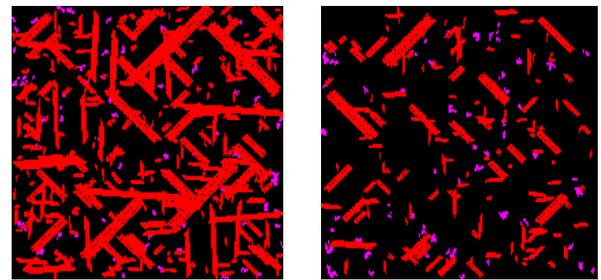


FIGURE 12. Predicted impact of Carbon co-implant on EOR defect evolution after spacer anneal. (a) reference sample, (b) with C co-implant.

Both physical modeling are in perfect agreement with the latest understanding of the physical mechanisms involved (15-17). Fig. 11 shows that the different impact of Carbon for n-type and p-type can be accurately simulated, as well as the impact on EOR defect evolution (see Fig. 12). An interesting feature can be seen from Fig. 13, which reveals the Carbon impact on both lateral and vertical diffusion in the case of PMOS technology.

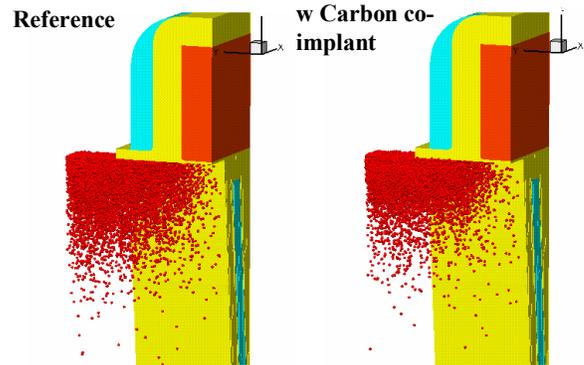


FIGURE 13. Predicted impact of additional Carbon co-implant in S/D extension on 3D boron atoms repartition for PMOS 45nm technology.

Based on the predictions of impurity co-implant, a design of experiments for 65nm-G PMOS/NMOS SD extension splits was conducted. Example of the comparison of electrical data of predicted simulations and actual experiment test data is shown in Fig. 14. These results clearly prove that kMC simulations can be directly applied for device design and optimization in the manufacturing process.

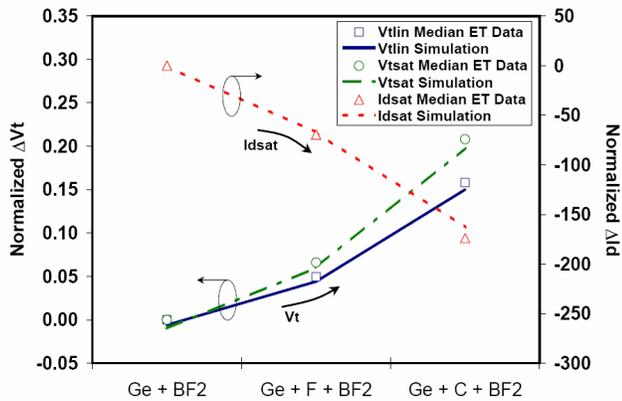


FIGURE 14. Comparison between predicted co-implant impact on 65nm-G PMOS device performance versus electrical data.

Finally, we conclude by presenting, in Fig. 15, a 3D atomistic process simulation of a 65nm SRAM cell. This opens new potential capabilities for linking process variability to critical circuit design.

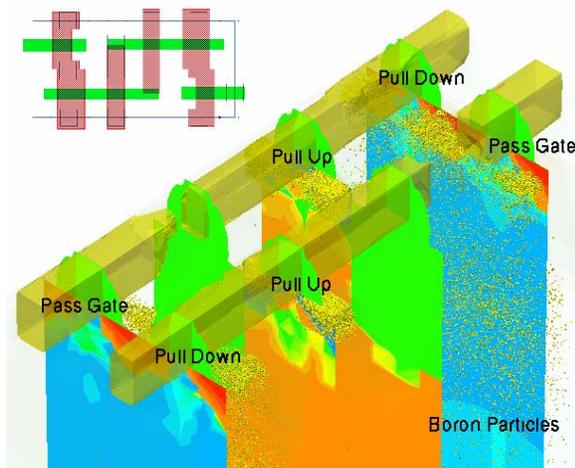


FIGURE 15. 3D atomistic and continuum profiles for 65nm SRAM.

Conclusions

This work showed that the design and optimization of nanoCMOS devices could be achieved from atomistic physics-based process modeling. We demonstrated that kMC DADOS could generate accurate 2D/3D profiles for present and future nanoCMOS devices, and also obtain remarkable prediction of device characteristics for a comprehensive series of novel co-implant processes. This extends the strength of TCAD in manufacturing for the prediction of future generations of nanoCMOS devices.

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