Analog-to-Digital Converters

By Wolfgang Reis

How do Analog-to-Digital converters work and What can you read out of the ADC specifications?

The Analog-to-Digital Converter (ADC) is probably the most important electronic component inside test-and-measurement equipment. ADCs convert voltages that represent real-world signals into bits that microprocessors and software use to manipulate test data and control test equipment. Even if you work on digital signals exclusively, you probably use an ADC in an oscilloscope to look at the analog characteristics of your signals.

ADCs come in several basic architectures, although many variations exist for each type. Different types of test equipment need different types of ADCs. For example, a digital oscilloscope needs high digitizing speeds but can sacrifice resolution.

A Digital Multimeter (DMM) needs fine resolution and can sacrifice high measurement speeds. General-purpose data-acquisition equipment usually falls between scopes and DMMs for sample speed and resolution. This type of equipment uses successive-approximation register (SAR) or sigma-delta converters. In addition to these both type of converters we will discuss in more detail, there are also Flash converters for very high speed applications and Integrating ADCs with high resolution and superior noise rejection.

Figure 1 provides a graph of resolution versus sample rate and shows where the basic ADC types fit on the graph.

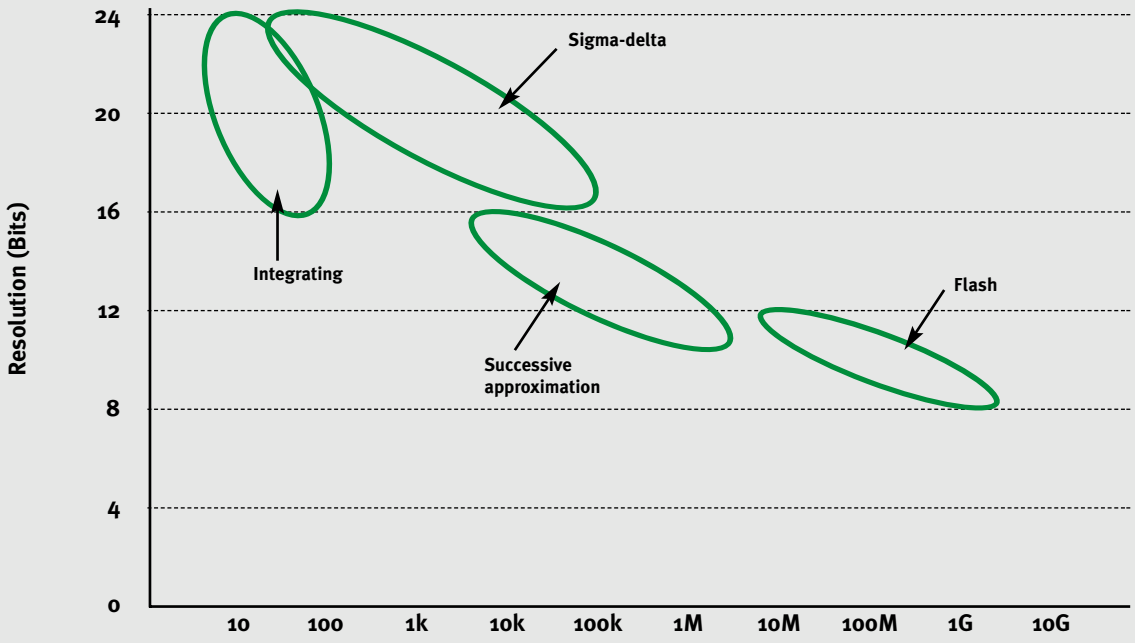


Figure 1: ADC Types - Resolution vs. Sample Rate

Flash Converters

Most high-speed oscilloscopes and some RF test instruments use flash ADCs because of their fast digitizing rate, which now reaches 5 Gsamples/s for off-the-shelf devices and 20 Gsamples/s for proprietary designs. The typical flash converter resolves analog voltages to 8 bits, although some flash converters can resolve 10 bits.

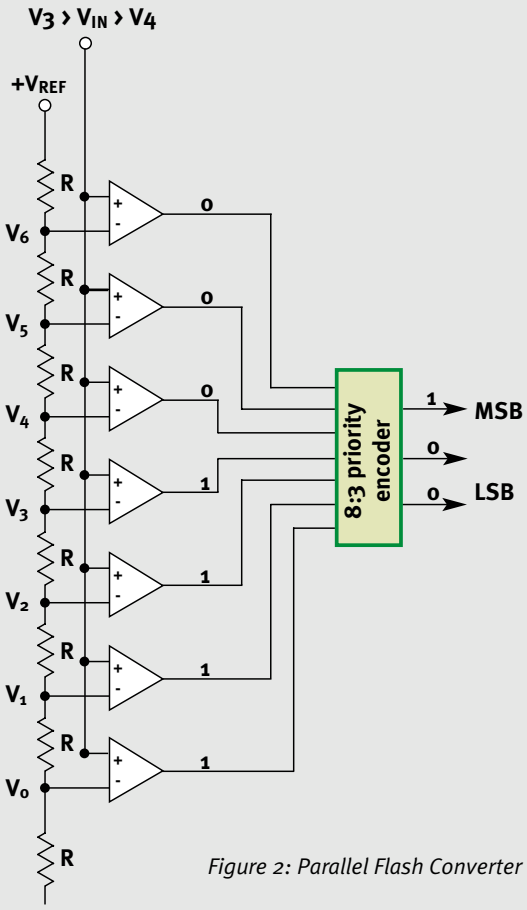


Figure 2: Parallel Flash Converter

Figure 2 shows a simplified block diagram for a parallel flash converter. For simplicity, a 3-bit converter is shown, but the concept extends to other resolutions. Parallel flash converters use a bank of comparators that compare the input voltage to a set of reference voltages across a resistor network. The voltages start at a value equal to that for one-half the least-significant bit (LSB) and increase in equal voltage increments equivalent to one LSB for each comparator. As a result, a 3-bit flash ADC requires 2^3–1, or seven, comparators. Each comparator's output represents one LSB. An 8-bit flash converter uses 255 (2^8–1) comparators.

As the input voltage increases, the comparators set their outputs to logic 1 starting with the lower-most comparator. Think of the converters as being like a mercury thermometer. As temperature increases, the mercury rises. Likewise, as the input voltage increases, comparators referenced to higher voltages set their outputs from 0 to 1. In Figure 2, the input voltage falls between V3 and V4, so the four lower comparators have logic-1 outputs while the upper three comparators have logic-0 outputs. A digital encoder circuit converts the comparator outputs into a 3-bit binary-weighted code.

Flash converters are fast, but they have drawbacks. Because they require so many comparators, flash ADCs consume considerable power, making them impractical for battery-powered equipment.

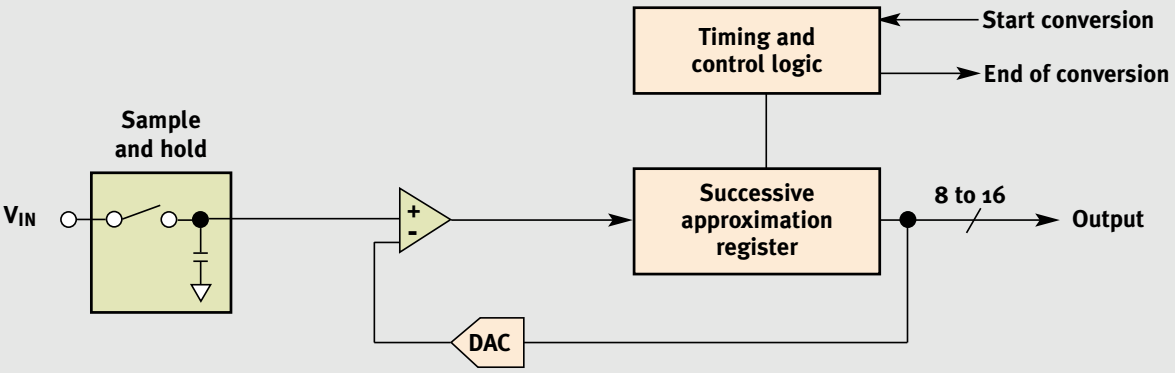
SAR Converters

When you need resolution from 12, 14, or 16 bits, but you don't need the speed of a Flash ADC and you want to use a lower cost device that draws less power, look for equipment that contains a Successive Approximation Register (SAR). SAR converters are by far the most popular ADCs in measurement products. If you use a PC plug-in data-acquisition board or PC-external data-acquisition system, you probably use an SAR converter.

Currently, SAR converters resolve voltages to 16 bits with sampling speeds of about 100 ksamples/s up to 1 Msamples/s.

At the start of a conversion, the SAR converter sets its successive-approximation register output so that all bits except the MSB produce logic 0. That sets the DAC's output (Figure 3) to one-half of the device full-scale input. The comparator sets its output based on the difference between the DAC output and the sampled voltage.

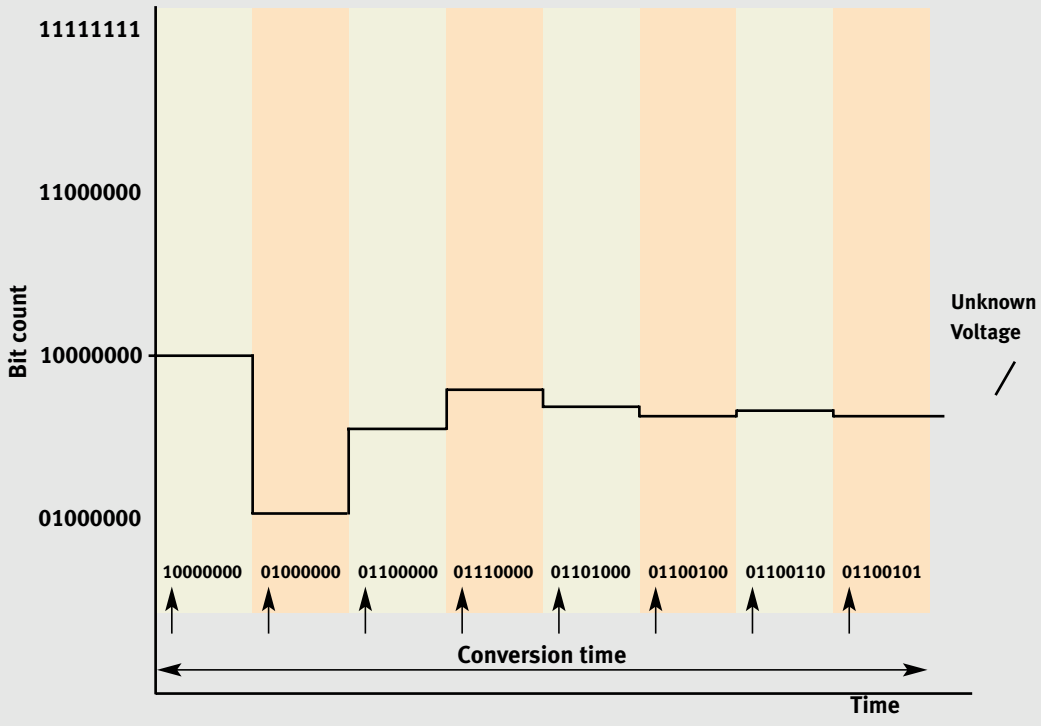
Figure 3: Successive Approximation Register (SAR) converters



For example, consider an 8-bit SAR converter (Figure 4). The register output starts at 10000000. If the input voltage is less than one-half of the ADC full range, then the comparator output goes (or stays) low. That forces the register output to 01000000, which changes the DAC output voltage to the comparator. If the comparator output stays low, then the register output changes to 00100000, and so on. SAR converters, therefore, need one cycle for each output bit, or N cycles for an N-bit converter.

A 16-bit SAR converter takes longer than twice the conversion time of an 8-bit SAR converter, because the output must settle to one bit in 65,536, where an 8-bit ADC needs to settle to one bit in 256.

Figure 4: SAR conversion



Sigma-Delta Converters

Many measurement applications don't need the conversion rates possible with SAR converters, but these applications need finer resolution. Sigma-delta ADCs can provide resolution as fine as 24 bits and they can trade resolution for speed. At 16 bits, you can get sample rates up to about 100 ksamples/s. At 24 bits, the ADC speed drops to around 1000 samples/s or lower, depending on the device.

Sigma-delta ADCs find use in data-acquisition systems and in vibration test equipment. Sigma-delta ADCs also find widespread use in weighting systems and temperature-measurement applications, which don't need high-speed sampling but often need resolution finer than 16 bits.

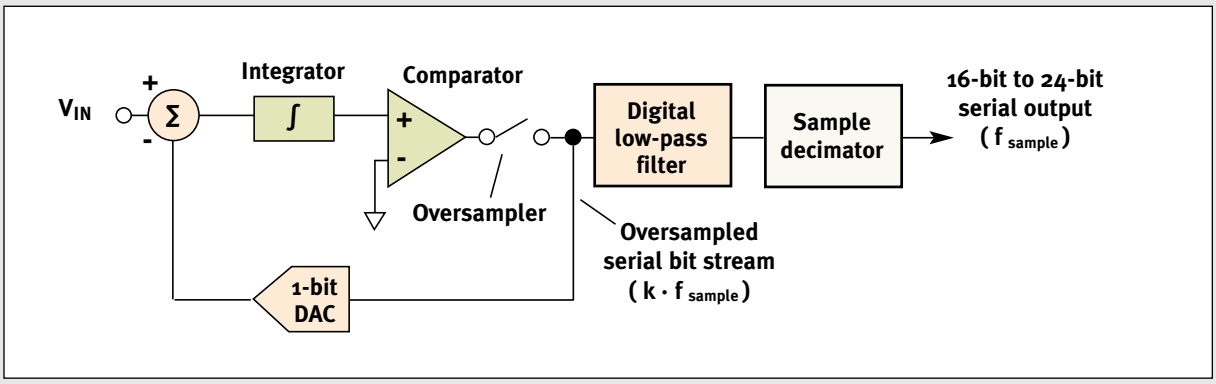
Sigma-delta ADCs are far more complex than other ADC types. The block diagram in Figure 5 shows the basic components of a sigma-delta ADC. A sigma-delta ADC with a 100-ksamples/s conversion rate that uses 128X oversampling will sample the incoming analog signal at 12.8 Msamples/s.

The oversampled analog signal goes through an integrator whose output drives a comparator (a 1-bit ADC) that, in turn, drives a 1-bit DAC in the feedback loop. Through a series of iterations, the integrator, comparator, DAC, and summing junction produce a serial bit stream that represents the oversampled input voltage.

Once digitized, the oversampled signal goes through a digital filter to remove frequency components at or above the Nyquist frequency, which is one-half of the ADCs output-sampling rate. A digital low-pass filter removes those high-frequency components, and a data decimator removes the oversampled data. In an ADC with 128X oversampling, the decimator will retain 1 bit for every 128 bits that it receives. The final output is a serial bit stream.

Because the internal digital filter in the sigma-delta ADC is an integral part of the conversion process, its settling time becomes a factor when you want to measure step functions. You may lose some important information because of the ADC sample rate. This settling time, or "latency," may be several clock cycles at the final output data rate.

Figure 5: Sigma-delta ADCs



Integrating ADCs

Finally there is another ADC architecture called integrating type or dual-slope ADCs. Digital Multi Meters use integrating ADCs because these instruments require high resolution with superior noise rejection. The concept behind the integrating ADC is far less complex than the sigma-delta ADC.

Figure 6 shows how the integrating ADC works. The sampled signal charges a capacitor for a fixed amount of time, usually one power-line cycle (50 Hz or 60 Hz). By integrating over one line cycle, any power-line noise integrates out of the conversion.

When the charging time ends, the ADC discharges the capacitor at a fixed rate while a counter counts the ADC output bits. A longer discharge time results in a higher count. As a result, V2 in Figure 7 produces a larger digital output value than V1 does.

Integrating ADCs work best in high-accuracy, fine-resolution systems because they remove any power-line frequency noise from the input signal. But removing that noise limits the converter's sample rate to about 30 samples/s for 60-Hz equipment. Integrating ADCs can run at higher sample rates, but as speed increases, noise immunity decreases.

ADC specifications

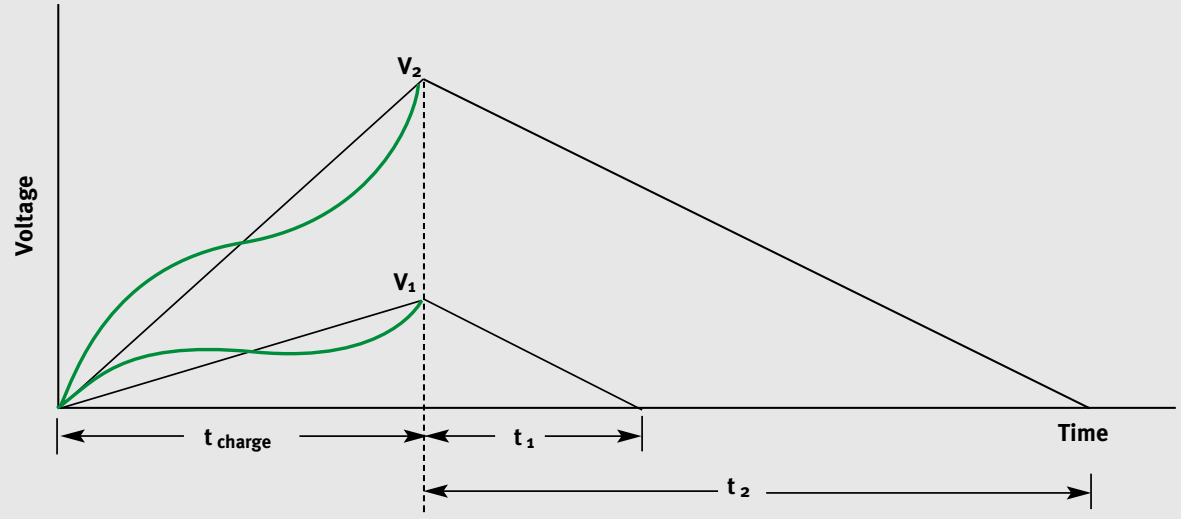
There are common terms used to describe analog-to-digital converters (ADCs), but a survey of the way ADC manufacturers specify the performance of ADCs in data sheets can be confusing. Understanding ADC specifications is essential in helping the engineer to choose the correct ADC for an application. ADCs convert an analog signal input to a digital output code. Due to process variations in integrated circuits and various sources of inaccuracies in the analog-to-digital conversion process, ADC measurements deviate from the ideal. ADC performance specifications quantify errors that are caused by the ADC itself.

ADC performance specifications are generally categorized in two ways: dc accuracy and dynamic performance. Generally, most applications use ADCs to measure

- a relatively static, dc-like signal (e.g., a temperature sensor or strain gauge voltage) or
- a dynamic signal (e.g., process a voice signal or tone detection).

The application determines which specifications the designer will consider the most important.

Figure 6: Integrating ADCs



Resolution

For an ADC, resolution is simply a measure of how many segments the input analogue range can be divided into (e.g, 8-bit ADC -› 2^8 = 256 segments). Resolution is NOT the same as accuracy. You could have a 12-bit ADC that is less accurate than an 8-bit ADC!

DC-Accuracy

Many signals remain relatively static, like that of a temperature sensor or pressure transducer. In such applications, the measured voltage is related to some physical measurement, and so the absolute accuracy of the voltage measurement is important. The ADC specifications that describe this type of accuracy are offset error, full-scale error, differential nonlinearity (DNL), integral nonlinearity (INL), and quantization error. These five specifications build a complete description of an ADC absolute accuracy.

One of the fundamental errors in ADC measurement is a result of the process of the data conversion itself: quantization error. This error cannot be avoided in ADC measurements. The quantization noise in a data conversion is dictated by the resolution of the measurement.

The Ideal ADC Transfer Function

The transfer function of an ADC is a plot of the input voltage to the ADC versus the codes output by the ADC. Such a plot is not continuous, but a plot of 2N codes, where N is the ADC resolution. If the codes were to be connected by lines (usually at code transition boundaries), the ideal transfer function would be a straight line.

A line drawn through the points at each code boundary would begin at the origin of the plot, and the slope of the plot for each supplied ADC would be the same (see Figure 7)

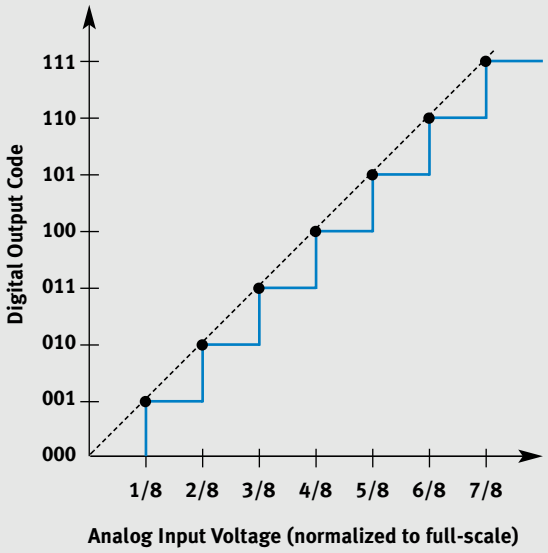


Figure 7: Ideal Transfer Function of a 3-Bit ADC

Figure 7 depicts an ideal transfer function for a 3-bit ADC with reference points at code transition boundaries. The output code will be its lowest (ooob) at less than 1/8 of the full-scale (the size of this ADC code width). Also note that the ADC reaches its full-scale output code (111b) at 7/8 of full-scale, not at the full-scale value. Thus, the transition to the maximum digital output does not occur at full-scale input voltage. The transition occurs at one code width (or LSB) less than full-scale input voltage (i.e., voltage reference

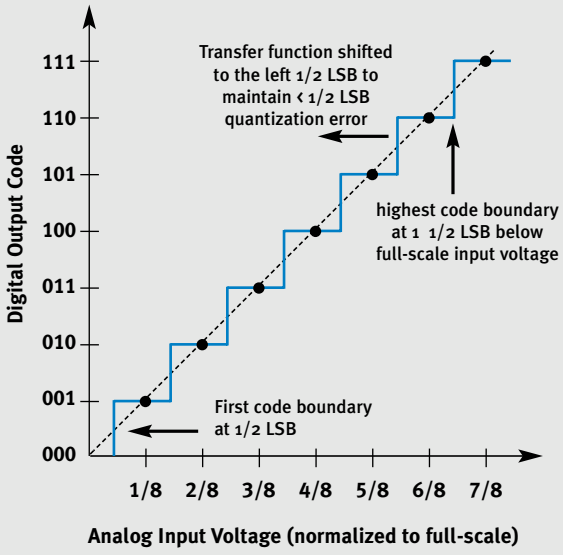


Figure 8: 3-Bit ADC Transfer Function with –1/2 LSB

voltage). The transfer function can be implemented with an offset of –1/2 LSB. This shift of the transfer function to the left shifts the quantization error from a range of (–1 to 0 LSB) to (–1/2 to +1/2 LSB).

Due to limitations in the elements used to fabricate an ADC on an integrated circuit, real-world ADCs will not have this perfect transfer function. It is these deviations from the perfect transfer function that define the dc-accuracy and are characterized by the specifications in a data sheet.

Offset Error

The ideal transfer function line will intersect the origin of the plot. The first code boundary will occur at 1 LSB . Offset Error can be observed as a shifting of the entire transfer function left or right along the input voltage axis, as shown in Figure 9. Thus, the offset error specification of an ADC includes 1/2 LSB of offset by design.

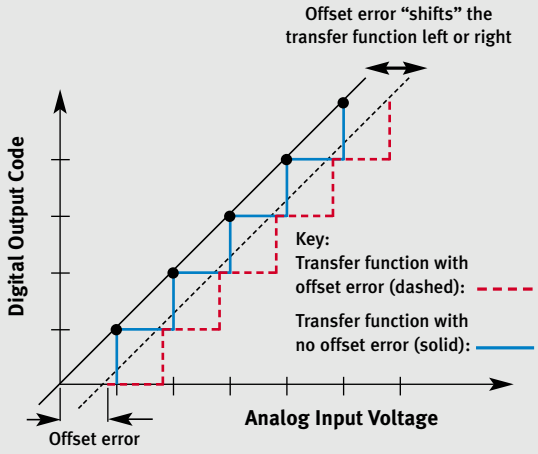


Figure 9: Offset Error

Full-Scale Error

Full-scale error is the difference between the ideal code transition to the highest output code and the actual transition to the output code when the offset error is zero. This is observed as a change in slope of the transfer function line as shown in Figure 10.

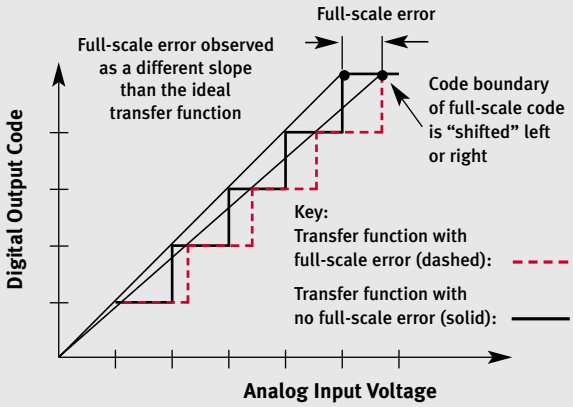


Figure 10: Full-Scale Error

Differential Nonlinearity

The size of each code width should be the same for an ADC. The difference in code widths from one code to the next is differential nonlinearity (DNL). The code width (or LSB) of an ADC is:

$$\text{LSB} = \frac{V_{REF}}{2^N}$$

where Vref is the voltage reference, and N is the ADC resolution.

The voltage difference between each code transition should be equal to one LSB. Deviation of each code from an LSB is measured as DNL. This can be observed as uneven spacing of the code "steps" or transition boundaries on the ADC's transfer function plot.

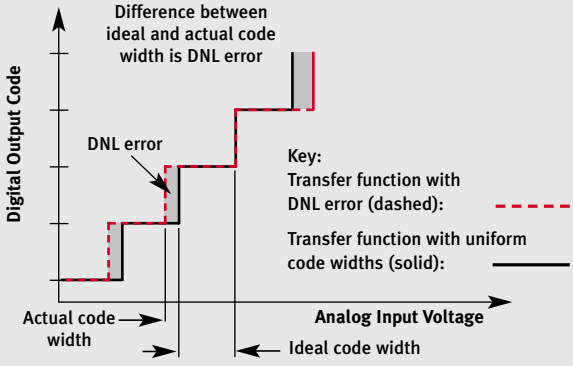


Figure 11: Differential Nonlinearity

Integral Non-Linearity Error

The integral nonlinearity (INL) is the deviation of an ADC transfer function from a straight line. This line is often a best-fit line among the points in the plot, but can also be a line that connects the highest and lowest data points (or endpoints). Measuring the voltage at which all code transitions occur and comparing them to the ideal determine INL. The difference between the ideal voltage levels at which code transitions occur and the actual is the INL error, expressed in LSBs .This is observed as the deviation from a straight-line transfer function.

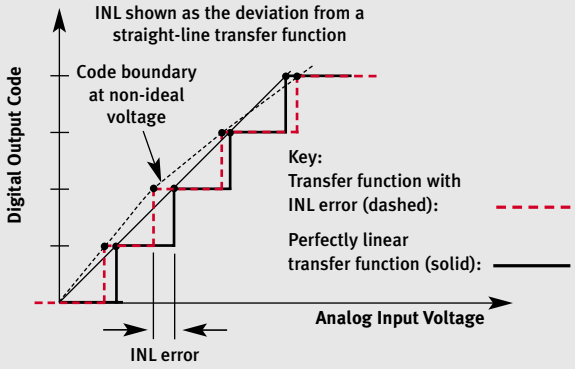


Figure 12: Integral Nonlinearity Error

Absolute Error

The absolute error is fully characterized by the offset, full-scale, INL, and DNL errors. Quantization error also affects accuracy, but it is inherent in the analog-to-digital conversion process and does not vary from ADC to ADC of equal resolution. Offset and full-scale errors can be minimized via calibration at the expense of reducing the dynamic range of the ADC and the production cost of the calibration process itself. Adding or subtracting a number to or from the ADC output codes can minimize offset error. Multiplying the ADC output codes by a correction factor can minimize full-scale error. Absolute error is less important in some applications such as closed-loop control, where DNL is most important.

Dynamic Performance

An ADC dynamic performance is specified using parameters obtained via frequency domain analysis. An ADC dynamic performance is typically measured by performing a Fast Fourier Transform (FFT) on the output codes of the ADC. This section discusses the ADC dynamic performance specifications using illustrations of typical FFTs. In Figure 13, the fundamental frequency is the input signal frequency. This is the desired signal to measure with the ADC. Everything else is noise (the unwanted signals) to be characterized with respect to the desired signal. This includes harmonic distortion, thermal noise, 1/f noise, and quantization noise. Some sources of noise may not be due to the ADC itself. For example, distortion and thermal noise originate from the external circuit at the input to the ADC.

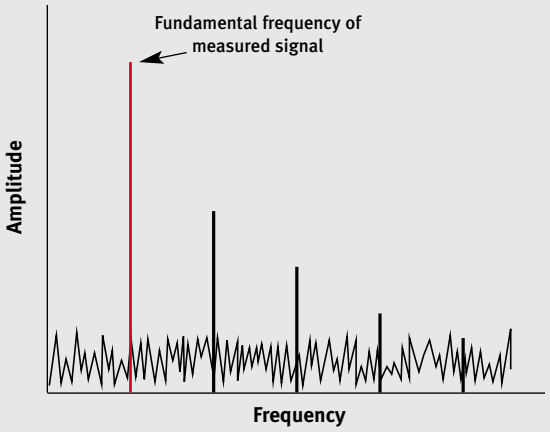


Figure 13: An FFT of ADC Output Codes

Signal-To- Noise Ratio

Signal-to-noise ratio (SNR) is the ratio of the rms power of the input signal to the rms noise power (excluding harmonic distortion), expressed in decibels (dB):

$$SNR(dB) = 20 \log \left[\frac{V_{signal(rms)}}{V_{noise(rms)}} \right]$$

This is a comparison of the noise to be expected with respect to the measured signal.

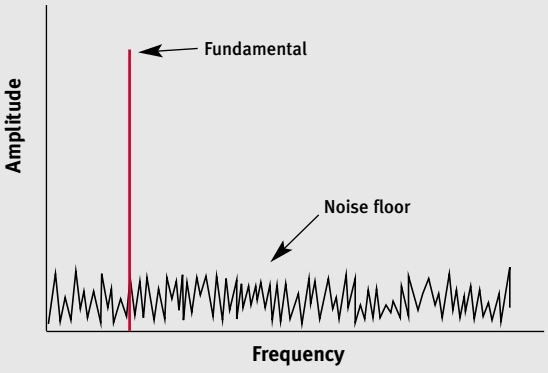


Figure 14: SNR - A Measure of the Signal Compared to the Noise Floor

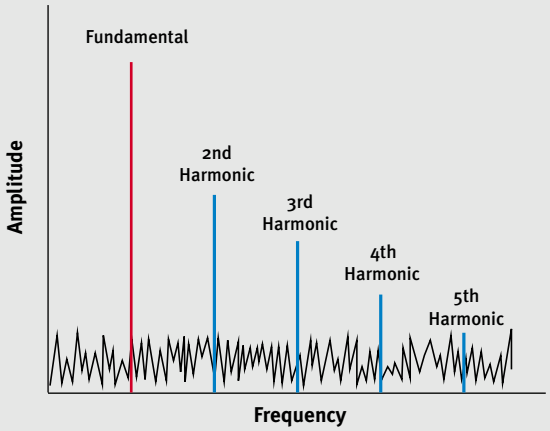


Figure 15: FFT Showing Harmonic Distortion

The noise measured in an SNR calculation does not include harmonic distortion but does include quantization noise. For a given ADC resolution, the quantization noise is what limits an ADC to its theoretical best SNR. The theoretical best SNR is:

$$SNR(db) = 6.02\,N + 1.76$$

where N is the ADC resolution.

Quantization noise can only be reduced by making a higher-resolution measurement (i.e., a higher-resolution ADC or oversampling). Other sources of noise include thermal noise, 1/f noise, and sample clock jitter.

Harmonic Distortion

Non-linearity in the data converter results in harmonic distortion when analyzed in the frequency domain. Such distortion is observed as "spurs" in the FFT at harmonics of the measured signal. See Figure 15.

This distortion is referred to as total harmonic distortion (THD), and its power is:

$$THD = 20 \log \left[\frac{\sqrt{V_2^{\,2} + V_3^{\,2} + \ldots\ldots V_n^{\,2}}}{V_1} \right]$$

The magnitude of harmonic distortion diminishes at high frequencies to the point that its magnitude is less than the noise floor or is beyond the bandwidth of interest.

Signal To Noise and Distortion

Signal-to-noise and distortion (SiNAD) offers a more complete picture by including the noise and harmonic distortion in one specification. SiNAD gives a description of how the measured signal will compare to the noise and distortion. SiNAD ratio is calculated:

$$SiNAD = 20 \log \left[\frac{V_1}{\sqrt{V_2^{\,2} + \ldots\ldots V_n^{\,2} + V_{noise}^{\,2}}} \right]$$

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the difference between the magnitude of the measured signal and the highest spur peak. This spur is typically a harmonic of the measured signal, but does not have to be. See Figure 16

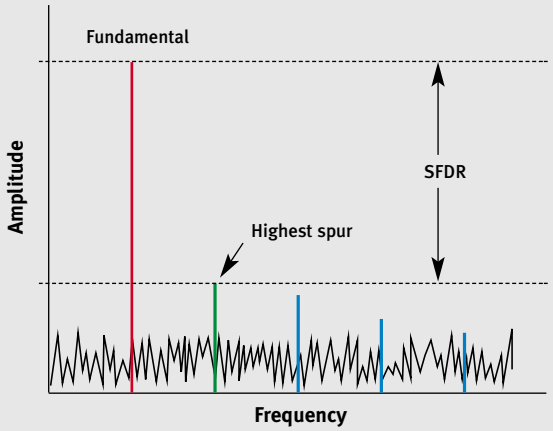


Figure 16: Spurious-Free Dynamic Range

Reading ADC Specification Numbers

The ADC specifications posted in data sheets serves to define the performance of an ADC in different types of applications. The engineer uses these specifications in order to define if, how, and in what way the ADC should be used in an application. Table 1 shows the specifications of the integrated ADC's in Silicon Laboratories superior Mixed-Signal MCUs.

Silicon Laboratories new C8051F064 Mixed-Signal MCU with two integrated 16-bit ADCs

After understanding ADC specifications this last section will introduce a new ADC product from Silicon Laboratories and demonstrate the state-of-art converter technology. The C8051F064 is definitely more than just an ADC, it is a mixed-signal MCU with two integrated 16-bit SAR converters (Single-ended or differential mode) that allow a maximum throughput of 1 Msamples/s. The voltage reference can be supplied from internal or external sources. The integrated DMA interface allows direct memory access from the ADC to the on-chip or external RAM. The MCU itself is a 8051-based core which runs 70% of the commands in a single cycle out of the internal FLASH memory (32k and 64k version). As it can be clocked as fast as 25MHz, the peak performance can reach 25 MIPS (million instructions per second). Finally several communication interfaces like two UARTs, SMBus (I2C compatible) and SPI make this a complete system on-chip.

The C8051F064 has industry-leading mixed-signal integration with great analog performance of the dual 16-Bit ADCs on-chip. The electrical characteristics in Figure 17 prove this performance, applying what explained above on ADC specifications.

To make performance tests ask WBC for the C8051F064 Evaluation kit. For 24.95 $ there is everything in hand to start.

The C8051F064EK evaluation kit contains a C8051F064 based evaluation board and comes complete with USB cables and full documentation. The evaluation kit includes analog testing software, per-

Table 1: Analog-to-Digital Converter Specifications

	C8051F300	C8051F330	C8051F005	C8051F060	C8051F350
Resolution	8-bit	10-bit	12-bit	16-bit	24-bit
Speed (sps)	500k	200k	100k	1M	1000
SINAD (dB)	48	55.5	66	89	2.4uV*
INL (LSB)	+ 0.5	+ 0.5	+ 0.5	+ 0.75	+ 15 ppm
DNL (LSB)	+ 0.5	+ 0.5	+ 1.0	+ 0.5	N/A
Offset	+ 0.6 LSB	0 LSB	+ 1 LSB	0.1mV	+ 1 ppm
Gain	+ 0.5 LSB	1 LSB	+ 3 LSB	0.008% FS	0.002%FS
Vref (V)	None	2.4	2.4	2.4	2.4

** Gain = 1, Output word rate = 10 Hz*

mitting users to easily test the analog performance (both dynamic and static) of the high precision, 16-bit 1Msps ADC integrated into the C8051F064.

The kit software package also includes Silicon Laboratories standard IDE development tools allowing the user to develop up to 2k bytes of user code.

VDD= 3.0 V, AV+ = 3.0 V, AVDD = 3.0 V, VREF = 2.50 V (REFBE=0), -40 to +85° unless otherwise specified					
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Units**
DC Accuracy					
Resolution			16		bits
Integral Nonlinearity (C8051F060/1/4/5/6/7)	Single- Ended Differential		± 0.75 ± 0.5	± 2 ± 1	LSB
Integral Nonlinearity (C8051F062/3)	Single- Ended Differential		± 1.5 ± 1	± 4 ± 2	LSB
Differential Nonlinearity	Guaranteed Monotonic		± 0.5		LSB
Offset Error			0.1		mV
Full Scale Error			0.008		% F.S.
Gain Temperature Coefficient			0.5		ppm/°C
Dynamic Performance (Sampling Rate = 1 Msps, AVDD, AV+ = 3.3 V)					
Signal-to-Noise Plus Distortion	Fin = 10 kHz, Single Ended		86		dB
	Fin = 100 kHz, Single Ended		84		dB
	Fin = 10 kHz, Differential		89		dB
	Fin = 100 kHz, Differential		88		dB
Total Harmonic Distortion	Fin = 10 kHz, Single Ended		96		dB
	Fin = 100 kHz, Single Ended		84		dB
	Fin = 10 kHz, Differential		103		dB
	Fin = 100 kHz, Differential		93		dB
Spurious-Free Dynamic Range	Fin = 10 kHz, Single Ended		97		dB
	Fin = 100 kHz, Single Ended		88		dB
	Fin = 10 kHz, Differential		104		dB
	Fin = 100 kHz, Differential		99		dB
CMRR	Fin = 10 kHz		86		dB
Channel Isolation			100		dB
Timing					
SAR Clock Frequency				25	MHz
Conversion Time in SAR Clocks		18			clocks
Track Hold Acquisition Time		280			ns
Throughput Rate				1	Msps
Aperture Delay	External CNVST Signal		1.5		ns
RMS Aperture Jitter	External CNVST Signal		5		ps
Analog Inputs					
Input Voltage Range	Single- Ended (AINn - AINnG)	0		VREF	V
	Differential (AIN0 - AIN1)	-VREF		VREF	V
Input Capacitance			80		pF

Figure 17: C8051F064 Electrical characteristics

To develop with the C8051F064 we suggest buying a development kit for 299 $.

The C8051F060DK development kit contains everything needed to develop applications with the C8051F060, F061, F062, F063, F064, F065, F066 and F067 MCUs. The kit includes the following items:

- *EC2 Serial Adapter*
- *Integrated Development Environment (IDE) CD with Macro-Assembler and C Compiler Interface*
- *Target/Prototyping PCB (C8051F060TB)*
- *RS-232 Cable and JTAG Ribbon Cable*
  Wall Mounted Power Supply (Country Specific)

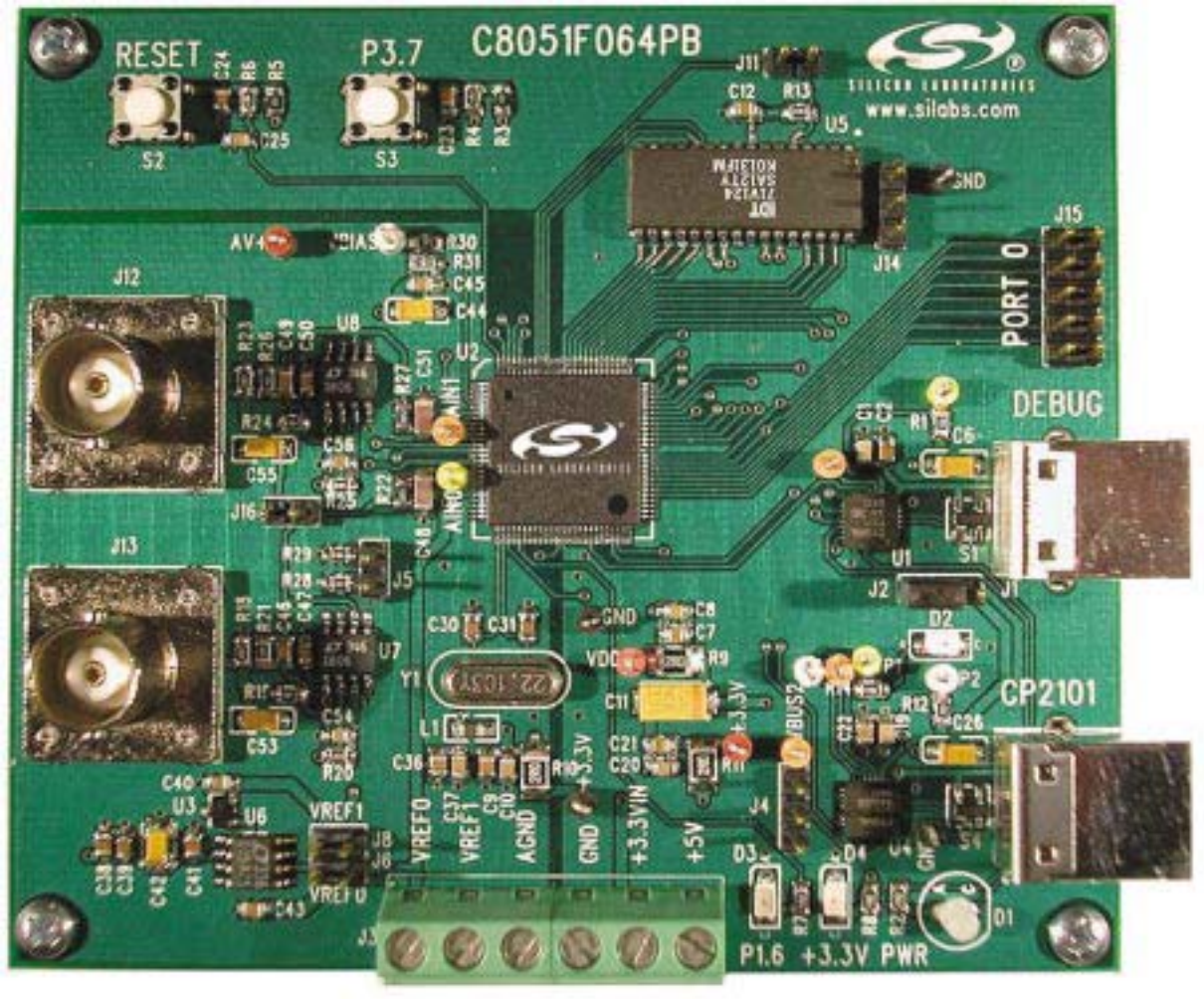


Figure 18: C8051F064EK Evaluation kit