AN693

Understanding A/D Converter Performance Specifications

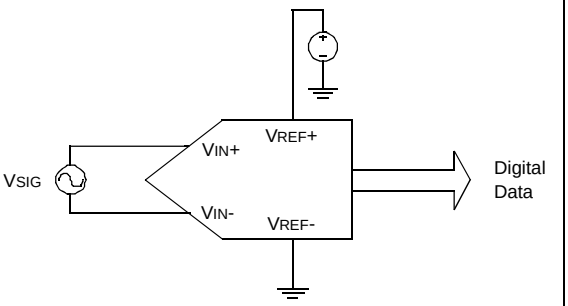
Authors: Steve Bowling
Microchip Technology Inc.

INTRODUCTION

The purpose of this application note is to describe the specifications used to quantify the performance of A/D converters and give the reader a better understanding of the significance of those specifications in an application. Although the information presented here is applicable to all A/D converters, specific attention is given to features of the stand-alone and PICmicro® A/D converters produced by Microchip Technology.

Figure 1 shows a block diagram of the typical A/D converter measurement circuit.

FIGURE 1: BASIC A/D CONVERTER MEASUREMENT CIRCUIT



THE IDEAL A/D CONVERTER

The ideal A/D converter produces a digital output code that is a function of the analog input voltage and the voltage reference input. The formula for the A/D converter digital output is given by Equation 1.

EQUATION 1: A/D OUTPUT

$$OutputCode = F.S. \times \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} = F.S. \times \frac{V_{IN}}{V_{REF}}$$

The analog input may be single-ended or differential. Differential inputs are especially useful in designs requiring 12 bits of accuracy or more and offer the advantage of cancelling common mode noise that may be present on the input lines.

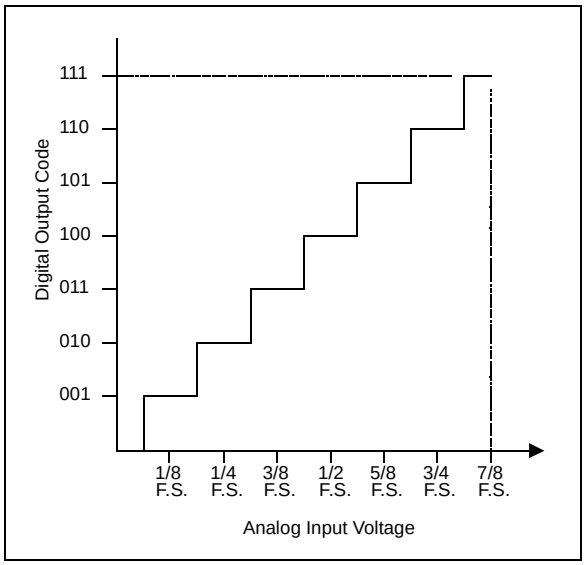
Some A/D converters have pseudo-differential inputs. For the pseudo-differential configuration, two pins (V_{IN}+ and V_{IN}-) are used for the signal input. The distinction between pseudo-differential inputs and standard differential inputs is that the signal on the V_{IN}- can only deviate a small range from the voltage of the V_{SS} supply rail. Although this restriction requires that a single-ended source is connected to the A/D converter, the input stage maintains the ability to cancel small common-mode fluctuations on the input pins.

The voltage reference for the A/D converter may be provided internally or by an external source. Since the accuracy of the measurement results is directly affected by the reference, it is important that the reference source be stable over time and temperature. For low cost converters, the reference input is often implemented as a single-ended input. In this case, one pin is used for the reference input and the input voltage range for the converter is determined by V_{SS} and V_{REF}. For higher performance converters, two voltage reference pins are typically provided. The input voltage range for these converters is determined by the voltage difference between V_{REF}+ and V_{REF}-. In either case, the voltage range for the reference inputs is usually restricted by the V_{DD} and V_{SS} power supply rails.

Although a “real world” A/D converter will have higher resolution, a theoretical 3-bit A/D converter will be used here to demonstrate the performance of the ideal converter and the various sources of error. Figure 2 shows the transfer function of the ideal 3-bit A/D converter. As the transfer function indicates, the ideal 3-bit A/D converter provides eight equally spaced digital output codes over the analog input voltage range.

Each digital output code represents a fractional value of the reference voltage. The largest value that can be obtained from the A/D converter is (N-1)/N, where N is the resolution in bits. Referring to Figure 2, the largest output value that the 3-bit A/D converter can produce is $7/8^{ths}$ of the full-scale reference voltage.

FIGURE 2: IDEAL A/D TRANSFER FUNCTION



Code Width

The width of a given output code is the range of analog input voltages for which that code is produced. The code widths are referenced to the weight of 1 least significant bit (LSb), which is defined by the resolution of the converter and the analog reference voltage. So 1 LSb = $V_{REF}/2^N$, where N is the number of bits of resolution. For example, if a 4.096 volt reference is used with a 12-bit converter, 1 LSb will have a weight of 4.096 $V/2^{12}$, or 1 mV. All codes will have a width of 1 LSb for an ideal A/D converter.

Resolution and Accuracy

Resolution and accuracy are terms that are often interchanged when the performance of an A/D converter is discussed. The resolution of an A/D converter is specified in bits and determines how many distinct output codes (2^N) the converter is capable of producing. For example, an 8-bit A/D converter produces 2^8, or 256, output codes.

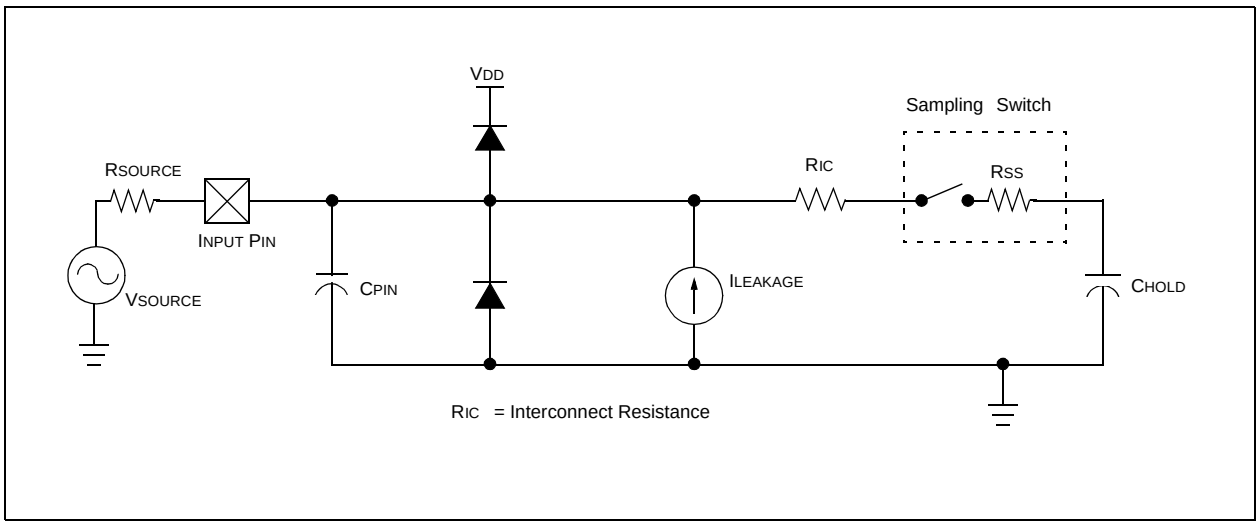
The accuracy of the A/D converter determines how close the actual digital output is to the theoretically expected digital output for a given analog input. In other words, the accuracy of the converter determines how many bits in the digital output code represent useful information about the input signal. The accuracy of the A/D converter is a function of its internal circuitry and noise from external sources connected to the A/D input.

In some cases, extra bits of resolution that are beyond the accuracy of the A/D converter can be beneficial. Delta-Sigma A/D converters, for example, can provide resolutions as high as 24 bits. A given 24-bit Delta-Sigma converter may only provide 16 bits of accuracy. In this case, the 8 LSb's represent random noise produced in the converter. However, these noise bits are used with digital filter algorithms to increase the useful measurement resolution at the expense of a lower sampling bandwidth.

Acquisition Time

A successive approximation (SAR) A/D converter will have a track and hold circuit at the analog input. Internally, the track and hold circuit is implemented as a charge holding capacitor that is disconnected from the analog input pin just before the A/D conversion begins. The holding capacitor must be given sufficient time to charge to its final value, or errors will be introduced into the conversion. The acquisition time that must be allowed is a function of the holding capacitor value, source impedance and internal resistances associated with the input circuit. Figure 3 shows a typical model for the analog input of a SAR A/D converter. The input model parameters will vary, so the designer should refer to the device data sheet to ensure that the proper acquisition time is provided based on the input circuit that is used in the design

FIGURE 3: TYPICAL SAR A/D CONVERTER ANALOG INPUT MODEL



Conversion Time

The conversion time is the time required to obtain the digital result after the analog input is disconnected from the holding capacitor. The conversion time is usually specified in A/D clock cycles and the minimum period for the clock is specified to obtain the specified accuracy for the A/D converter.

CODE TRANSITION POINTS

The transition points of the A/D converter are the analog input voltages at which the output code switches from one code to the next. For an ideal A/D converter, these transition points would occur at distinct, evenly spaced locations. In the real world, however, these transition points are not clearly defined due to sources of noise in the A/D converter. As an example, assume that an analog input voltage connected to the input of an A/D converter is adjusted until a constant output code is obtained. If the voltage is slowly increased or decreased from this point, there will be a range of analog input voltages that sometimes produces the first code or the next successive code in the transfer function. This range of analog inputs that produces either code is referred to as the code transition region and can be expressed statistically by averaging the results of many conversions. The code transition point is defined as the analog input level for which the probability of producing either output code is 50 percent. It is important that the code transition points are accurately determined, since the error specifications for the A/D converter are derived from them.

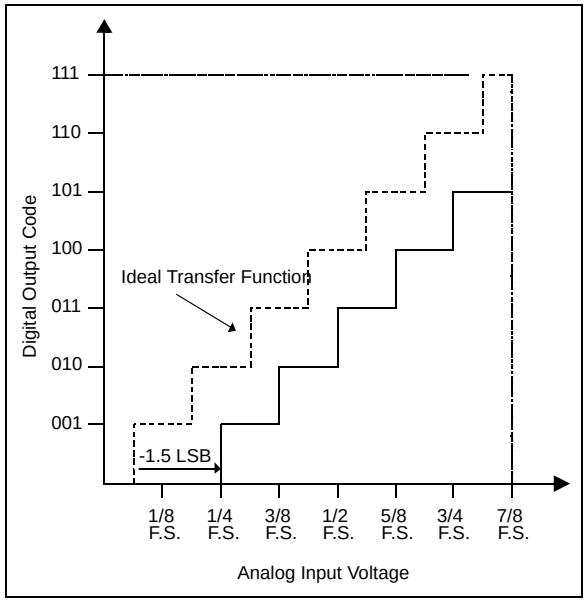
DC SPECIFICATIONS

The DC specifications for the A/D converter tell the designer how the device performs for steady-state analog inputs. These specifications are particularly important in instrumentation applications where the A/D converter is used to measure slowly varying physical events such as temperature, pressure or weight.

Offset Error

Offset error is defined as a deviation of the code transition points that is present across all output codes. This has the effect of shifting the entire A/D transfer function to the right or left as shown in Figure 4. The offset error is measured by finding the difference between the actual location of the first code transition and the desired location of the first transition. The offset error is measured at the first code transition, since contributions from other sources of error will be minimal at this point in the transfer function. Once the offset error has been determined, it can easily be subtracted from the digital output code so the correct conversion result is obtained. Referring to Figure 4, this transfer function shows that the converter has -1.5 LSb of offset error.

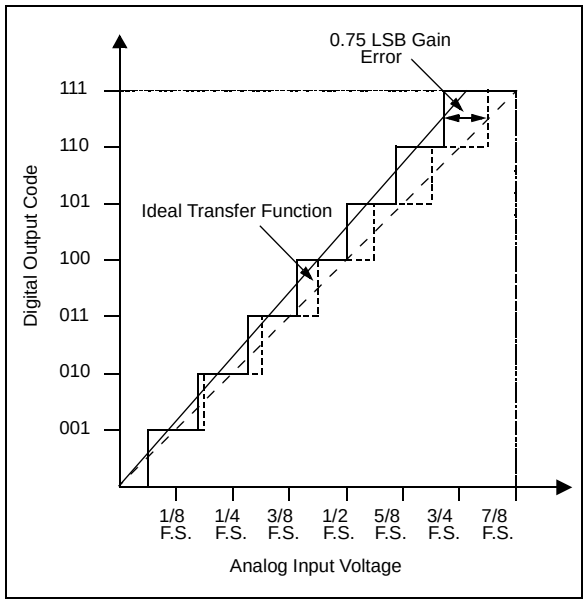
FIGURE 4: OFFSET ERROR IN THE A/D TRANSFER FUNCTION



Gain Error

The gain error determines the amount of deviation from the ideal slope of the A/D converter transfer function. Before the gain error is determined, the offset error is measured and subtracted from the conversion result. The gain error can then be determined by finding the location of the last code transition and then comparing that location to the ideal location. Figure 5 shows an example of gain error in the A/D transfer function.

FIGURE 5: GAIN ERROR IN THE A/D TRANSFER FUNCTION



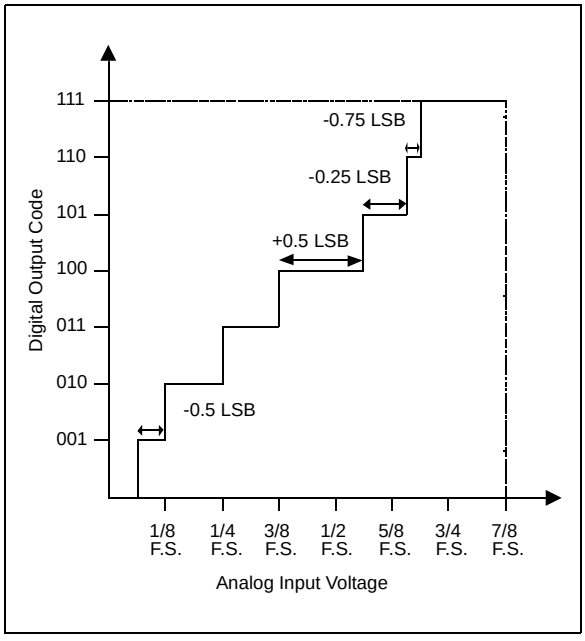
Gain error is easily compensated for in the digital measurement system by multiplying the conversion result by the necessary scaling factor. For the designer that

prefers a screwdriver and trim-pots, gain or attenuation can always be applied in the analog signal path to correct the A/D gain error.

Differential Nonlinearity

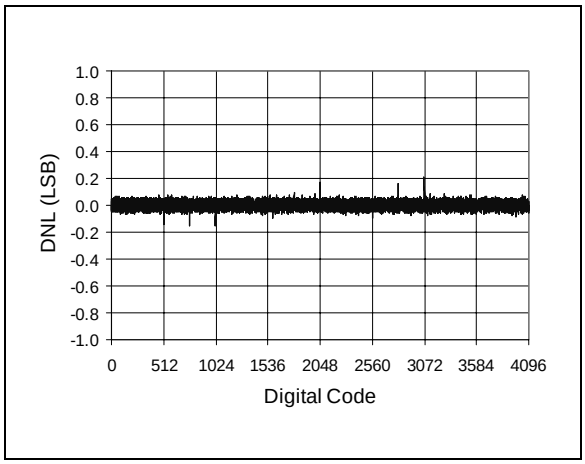
In the ideal A/D converter transfer function, each code has a uniform width. That is, the difference in analog input voltage is constant from one code transition point to the next. Differential nonlinearity, or DNL, specifies the deviation of any code in the transfer function from an ideal code width of 1 LSb. The DNL is determined by subtracting the locations of successive code transition points after compensating for any gain and offset errors. A positive DNL implies that a code is longer than the ideal code width, while a negative DNL implies that a code is shorter than the ideal width. Figure 6 shows an example of DNL errors in the A/D transfer function.

FIGURE 6: DNL ERRORS IN THE A/D TRANSFER FUNCTION



The DNL information may be provided to the designer in two ways. First, the maximum positive and negative DNL values are usually provided. Second, the DNL for each code may be provided in a graphical format. Graphical DNL data can give the designer good information regarding the 'quality' of the A/D converter. For example, a SAR A/D converter uses an array of capacitors and a comparator to determine the value of each bit in the conversion result. Imperfections of the individual capacitors will produce periodic fluctuations in the graphical DNL data. Figure 7 shows a graphical example of DNL vs. digital code.

FIGURE 7: DNL VS. DIGITAL CODE EXAMPLE



The DNL for any code cannot be less than '-1'. In fact, a DNL value of '-1' implies that a particular code does not exist at all. In other words, there is no analog input voltage that will produce the particular code.

Strictly speaking, the designer should expect that one or more codes may be missing in the transfer function if a value of -1 is specified as the minimum DNL for a particular A/D converter. However, the specifications may state that the A/D converter has a minimum DNL of -1 and will also indicate that the converter has 'no missing codes' for stated operating conditions. In this case, the minimum DNL of -1 is specified to ensure proper testing guard-bands and the probability that the designer will see a device with the actual minimum DNL near -1 is extremely low.

Integral Nonlinearity

Integral nonlinearity, or INL, is a result of cumulative DNL errors and specifies how much the overall transfer function deviates from a linear response. INL is sometimes simply referred to as the linearity of the converter. The INL specification tells the designer the best accuracy that the A/D converter will provide after calibrating the system for gain and offset. INL can be measured in two ways.

The first method used to determine INL is the end-point method. For the end-point method, the locations of the first and last code transitions for the converter are determined and a linear transfer function based on the endpoints is derived. The end-point nonlinearity is determined by finding the deviation from the derived linear transfer function at each code location.

The second method used to determine INL is the best-fit method. The best-fit response is found by manipulating the gain and offset for the measured transfer function, comparing against a linear transfer function, and balancing the total positive and negative deviations.

Figure 8 shows a comparison of linearity measurement methods for the same A/D converter. As the transfer functions indicate, the end-point method provides more conservative results, so the designer should always determine the method used to specify the INL.

The maximum positive and negative INL are usually specified for stated operating conditions. Furthermore, graphs indicating the INL for each code are sometimes given in the device data sheet. Like DNL graphical data, the INL graphical data can be used to analyze the quality of the A/D converter. Figure 9 shows a graphical example of INL vs digital code.

FIGURE 8: INL ERROR IN THE A/D TRANSFER FUNCTIONS

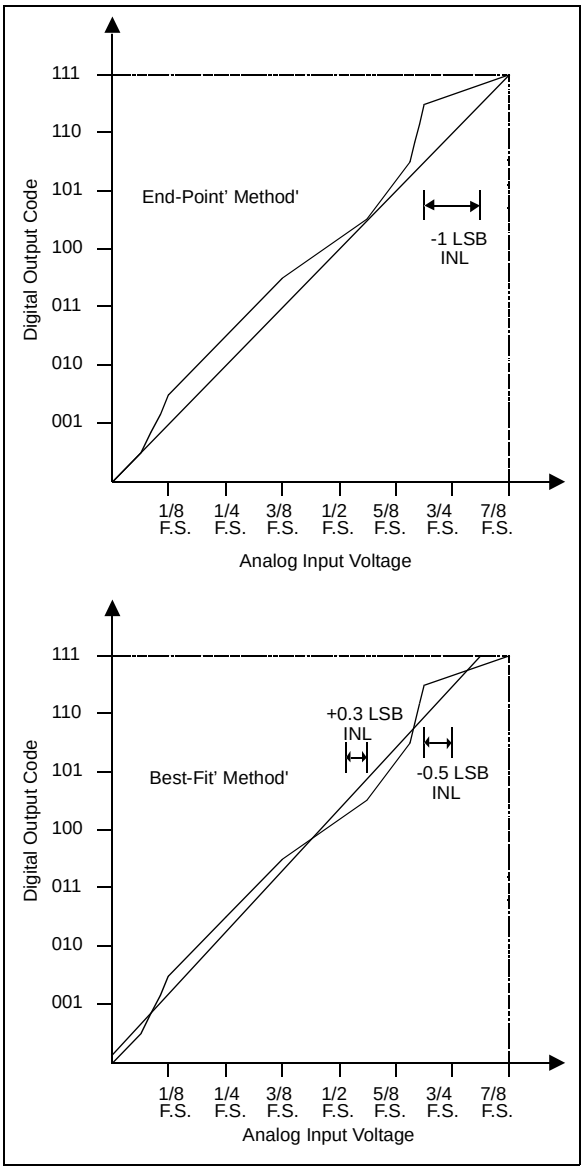
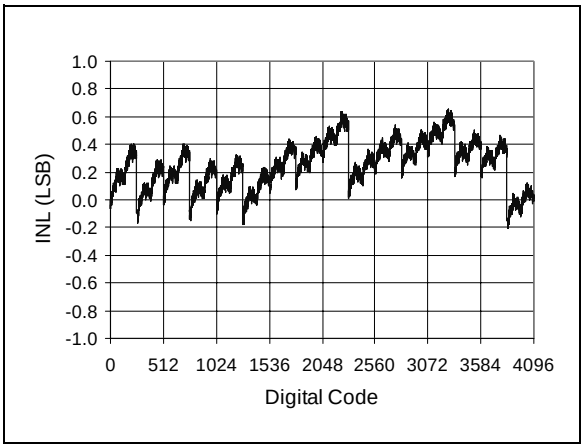


FIGURE 9: INL VS. DIGITAL CODE EXAMPLE



Absolute Error

The absolute error is specified for some A/D converters and is the sum of the offset, gain, and integral non-linearity errors. Stated differently, this is the amount of deviation from the ideal A/D transfer function without compensating for gain or offset errors. The absolute error is also called the total unadjusted error. This error specification gives the designer details of the worst-case A/D converter performance without any form of error compensation.

Monotonicity

An A/D converter is said to be monotonic if, for increasing (decreasing) analog input, the digital output code either increases (decreases) or stays the same. Monotonic behavior does not guarantee that there will be no missing codes. Monotonic behavior is an especially important characteristic for A/D converters used in feedback control loops since non-monotonic response can cause oscillations in the system.

AC SPECIFICATIONS

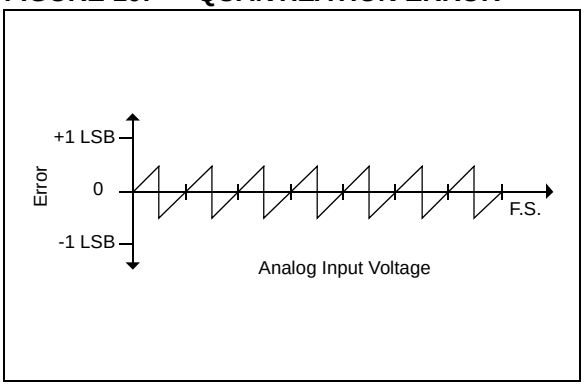
For applications where the signal is steady-state or has an extremely low frequency compared to the A/D converter sampling frequency, DC error specifications have the most significance. When the signal frequency is increased, however, other measures must be used to determine the performance of the A/D converter. In this case, the performance of the A/D converter in the frequency domain becomes significant to the designer. Imperfections of the A/D converter introduce noise and distortion into the sampled output. In fact, even the ideal A/D converter introduces errors into the sampled AC signal in the form of noise. The AC specifications tell the designer how much noise and distortion has been introduced into the sampled signal and the accuracy of the converter for a given input frequency and sampling rate.

Signal-to-Noise Ratio

If an AC signal is applied to an ideal A/D converter, noise present in the digitized output will be due to quantization error.

For the ideal converter, the maximum error for any given input will be +/- ½ LSb. If a linear ramp signal is applied to the converter input and the output error is plotted for all analog inputs, the result will be a sawtooth waveform with a peak-to-peak value of 1 LSb as shown in Figure 10.

FIGURE 10: QUANTIZATION ERROR



The root-mean-square (RMS) amplitude of the error output can be approximated by Equation 2.

EQUATION 2: MINIMUM RMS QUANTIZATION ERROR

$$ERROR_{RMS} = \frac{1}{\sqrt{12}} \bullet 1\,LSb$$

The maximum theoretical signal-to-noise ratio (SNR) for an A/D converter can be determined based on the RMS quantization error determined above. If a full-scale sine wave is applied to the input of the A/D converter, the maximum theoretical SNR is given by Equation 3, where N is the resolution of the A/D converter in bits.

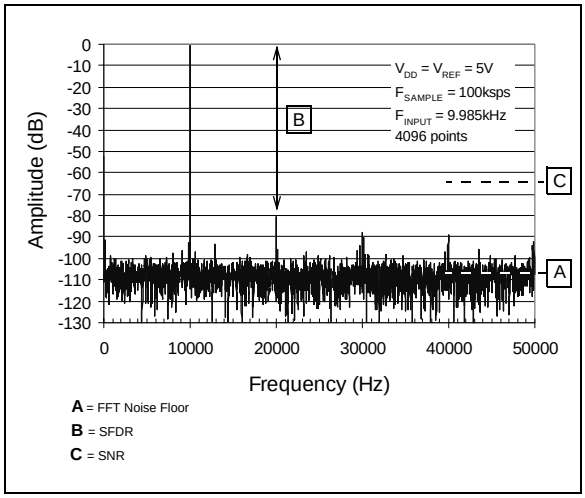
EQUATION 3: MAXIMUM A/D SNR

$$SNR = 6.02 \bullet N + 1.76dB$$

The above formula assumes that the signal noise is measured over the entire usable bandwidth of the A/D converter (0 - fs/2). For the case of oversampling where the signal bandwidth is less than the Nyquist bandwidth, the theoretical SNR of the A/D converter is increased by 3 dB each time the sampling frequency (fs) is doubled.

The performance of an actual A/D converter can be measured in the frequency domain by applying a sinusoidal input and performing an FFT analysis of the converter output data. Care must be taken, however, to ensure that the noise and distortion produced by the A/D converter is accurately determined. The quantization noise introduced into the sampled signal does not necessarily have a white noise spectrum and is a function of the input signal. If the sampling frequency is chosen to be an integer multiple of the signal input frequency, for example, peaks may occur in the FFT output data at harmonics of the input signal frequency due to a high degree of correlation with the quantization noise. In practice, most signals contain multiple frequencies, so the quantization noise will be randomly dispersed throughout the FFT spectrum. Figure 11 shows example FFT data taken from a 12 bit A/D converter. Note the choices of input signal frequency and sampling frequency. You can also observe the peaks in the spectrum at harmonics of the input signal.

FIGURE 11: EXAMPLE FFT SPECTRUM FOR AN A/D CONVERTER



The FFT spectrum obtained from the A/D converter will have a noise floor that is a function of N, data resolution in bits, and M, the number of points in the FFT data. For a set of M-point FFT data, the level of the FFT noise floor can be determined using Equation 4. In Figure 11, Label 'A' indicates the level of the noise floor.

EQUATION 4: FFT NOISE FLOOR

$$6.02 \bullet N + 1.76dB - 10 \bullet \log_{10}\left(\frac{M}{2}\right)$$

To find the actual SNR of the A/D converter, a sine wave with a level just below full-scale is applied to the input. The SNR is determined by finding the ratio of the RMS level of the input signal to the RMS value of the root-sum-square of all noise components in the FFT analysis, except for the DC component and harmonics of the input. Referring to Figure 11, Label 'C' indicates the SNR of the A/D converter. In practice, only the first several harmonics of the input are eliminated from the SNR calculation, since the higher order harmonics are usually insignificant when compared to the FFT noise floor.

Signal-to-Noise Ratio plus Distortion

The signal-to-noise ratio plus distortion, or SINAD, is measured with a sinusoidal input near full-scale applied to the A/D converter. The SINAD is found by computing the ratio of the RMS level of the input signal to the RMS value of the root-sum-square of all noise and distortion components in the FFT analysis, except for the DC component. The SINAD value is an especially useful measure of performance, because it includes the effect of all noise, distortion and harmonics introduced by the A/D converter.

Effective Number of Bits

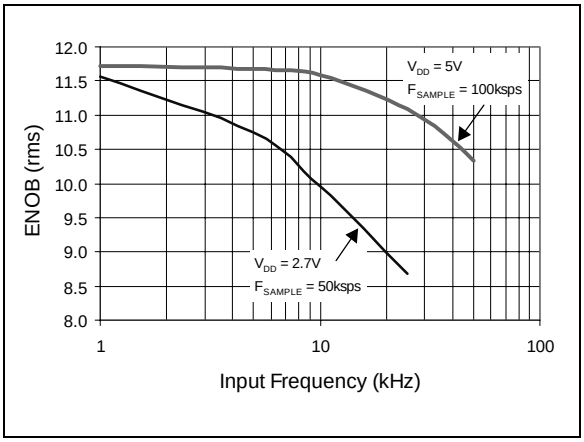
The effective number of bits (ENOB) value for an A/D converter is computed by substituting the measured SINAD value into the equation that describes the SNR for an ideal A/D converter and solving for N, the number of bits. Equation 5 shows the calculation for ENOB.

EQUATION 5: ENOB

$$ENOB = \frac{SINAD - 1.76dB}{6.02}$$

The ENOB is usually presented for a range of input frequencies and tells the designer how accurate the converter is as a function of input frequency and the chosen sampling rate. Figure 12 shows a graphical example of ENOB data taken from an A/D converter. Note that the sampling frequency and operating conditions have been specified.

FIGURE 12: EXAMPLE ENOB DATA



Total Harmonic Distortion

The total harmonic distortion value, or THD, is the RMS value of the root-sum-square of the harmonics produced by the A/D converter relative to the RMS level of a sinusoidal input signal near full-scale. In practice, only the first several harmonics of the input signal are included in the THD measurement, because greater-order harmonics are insignificant compared to the noise floor in the measured FFT output.

Total Harmonic Distortion plus Noise

Total harmonic distortion plus noise, or THD+N, is the RMS value of the root-sum-square of the harmonics and noise produced by the A/D converter relative to the RMS level of a sinusoidal input near full-scale. THD+N does not necessarily include all data from the FFT analysis. For a valid THD+N specification, the noise bandwidth must be specified. If the noise bandwidth is taken over the entire usable bandwidth of the A/D converter (0 - fs/2), then the THD+N measurement provides the same results as SINAD.

Spurious Free Dynamic Range

The spurious free dynamic range, or SFDR, is the ratio of the level of the input signal to the level of the largest distortion component in the FFT spectrum. This specification is important because it determines the minimum signal level that can be distinguished from distortion components. Label ‘B’ in Figure 11 shows the SFDR for the example A/D converter measurement data.

USING THE A/D CONVERTER

The following sections give the reader some insight on A/D measurement techniques. For more information, references to other Microchip Technology application notes have been provided at the end of this document. In addition, many other application notes that use the A/D converter are available from the Microchip Technology website.

Interpreting the Specifications

The designer should always review the specifications carefully to make sure the selected A/D converter is actually a good match for the application. While this may seem painfully obvious, a little 'reading between the lines' never hurts.

The importance of each specification will vary from application to application. For example, consider a digital weight measurement system that will be powered from a 3V supply. The weight applied to the load cell is going to be more or less constant, so the DC error specifications have the most significance here. The DC error specifications, for example, may look great at 5V, but questionable at the supply voltage required. Furthermore, let's assume that the scales are to be located in a harsh environment. In this case, it's wise to check the gain, offset and linearity specifications over the range of temperatures for which the device is expected to operate.

As another design example, consider an A/D converter to be used in a vibration signature analysis system. In many industrial applications, the outputs from vibration transducers attached to machinery are sampled and the data is stored in RAM for FFT analysis. By analyzing the location and amplitude of principal vibration components in the frequency domain, the machinery can be tested for faults such as cracks in the structure or worn bearings, for example. In this type of applica-

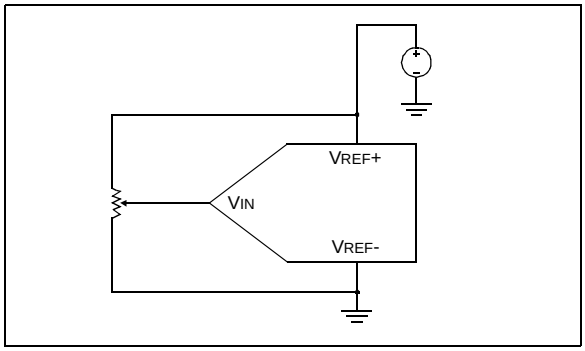
tion, the AC performance parameters will have much greater significance. The SFDR, for example, will determine the minimum vibration level that can be distinguished by the A/D converter. The AC performance parameters vary over frequency, so the designer should always check the performance at the maximum frequency of interest and the desired sampling rate.

Absolute vs. Ratiometric Measurements

An absolute measurement is a measurement that compares the analog input voltage against the A/D converter reference voltage, which may be external or internal. In order for the measurement result to be accurate, the reference source must be stable over time and temperature.

In contrast, a ratiometric measurement provides a result that is the ratio of the reference voltage. This is accomplished by using the reference voltage as a source of excitation for the analog input source. A simple example that demonstrates a ratiometric measurement consists of a potentiometer connected to the analog input of an A/D converter as shown in Figure 13.

FIGURE 13: RATIOMETRIC CIRCUIT



The potentiometer is connected across the power supply rails, which are also used as the reference inputs for the A/D converter. The output of the potentiometer is given by Equation 6, where x denotes the voltage division ratio of the potentiometer.

EQUATION 6: POTENTIOMETER OUTPUT

$$V_O = (V_{DD} - V_{SS}) \bullet x$$

The digital output of the A/D converter, as stated earlier, is given by Equation 7.

EQUATION 7: DIGITAL OUTPUT OF A/D

$$OutputCode = F.S. \times \frac{V_{IN}}{V_{REF}}$$

Finally, the reference voltage for the converter is given by Equation 8

EQUATION 8: REFERENCE VOLTAGE OF A/D

$$V_{REF} = V_{REF+} - V_{REF-} = V_{DD} - V_{SS}$$

If the expressions for the voltage reference and potentiometer output are substituted into the expression for the A/D output, the result is given by Equation 9.

EQUATION 9: A/D RESULT

$$\begin{aligned} OutputCode &= F.S. \times \frac{V_{IN}}{V_{REF}} \\ &= F.S. \times \frac{\cancel{(V_{DD} - V_{SS})} \bullet x}{\cancel{(V_{DD} - V_{SS})}} \\ &= F.S. \bullet x \end{aligned}$$

This equation for the digital output shows that the ratiometric measurement is not a function of the voltage reference source. Since the conversion result only represents a percentage of full-scale, a stable reference source is not critical for accuracy of the conversion.

Performing Conversions in Sleep

All Microchip Technology microcontrollers (MCUs) that contain an A/D module have the unique ability to perform conversions with the MCU in SLEEP mode. In this mode of operation, all system operation is halted and the system oscillator is shut down to minimize the effects of digital noise on the conversion.

To perform a conversion in SLEEP, the user must select the internal A/D RC oscillator option for the A/D clock source. When the RC clock source is selected for the A/D converter, the MCU will wait one extra instruction cycle before performing the conversion so the SLEEP instruction may be executed.

One of three possible actions can occur when the conversion is finished. First, if A/D interrupts are enabled, the device will wake-up from SLEEP and continue execution at the next program instruction. Secondly, if global interrupts are also enabled on wake-up, the MCU will continue operation at the interrupt vector address. Finally, if A/D interrupts are not enabled, the A/D module will be powered down to minimize current consumption and the device will remain in SLEEP mode.

Obtaining the Best System Performance

The performance of any A/D converter can be crippled by a poor system design. It is essential, therefore, that the designer use proper analog design techniques for an application. Particular attention should be given to the power supply, grounding and PCB layout. For more information on this topic, references to other Microchip application notes are given at the end of this document.

REFERENCES FOR FURTHER READING

There are many other application notes available from the Microchip website that will provide you with technical assistance for your A/D converter application.

- AN688 - Layout Considerations for 12-bit A/D Converter Applications
- AN699 - Anti-aliasing, Analog Filters for Data Acquisition Systems
- AN719 - Interfacing Microchip's MCP3201 Analog to Digital Converter to the PICmicro® Microcontroller

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

DNV Certification, Inc. USA — ANSI-RAB QMS ACCREDITED — DNV MSC The Netherlands Accredited by the RvA — DNV — ISO 9001 / QS-9000 REGISTERED FIRM

Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-6766200 Fax: 86-28-6766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

Hong Kong
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-334-8870 Fax: 65-334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Arizona Microchip Technology Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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