Low-Power Pipelined ADC Design for Wireless LANs

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Block Diagram of the ADC

Analog Input

Stage #1

Stage #2

Stage #8

Stage #9

Even Samples

Digital Delay & Correction Logic

Odd samples

Stage #1

Stage #2

Stage #8

Stage #9

Digital Delay & Correction Logic

MUX

Digital Output
Simplified Pipeline Stage

\[
\begin{align*}
V_{\text{in}} & \rightarrow +V_{\text{ref}}/4 \rightarrow +V_{\text{ref}}/4 \rightarrow \Phi_1 \rightarrow \Phi_2 \rightarrow C_1 \rightarrow (C_s) \rightarrow \Phi_2 \rightarrow \Phi_1 \rightarrow C_2 \rightarrow (C_s) \rightarrow V_{\text{res}} \\
& \rightarrow \text{Digital Output} \\
& \rightarrow +V_{\text{ref}} \rightarrow 0 \rightarrow -V_{\text{ref}} \\
& \rightarrow \text{1.5-bit Flash ADC} \\
& \rightarrow \text{1.5-bit DAC} \\
& \rightarrow V_{\text{res}} \rightarrow \text{Output}
\end{align*}
\]

Transfer function

\[
\begin{align*}
& +V_{\text{ref}} \quad 00 \quad 01 \quad 11 \\
& +V_{\text{ref}}/2 \quad 0 \quad \text{Digital Output} \quad 0 +V_{\text{ref}}/4 \\
& 0 \quad -V_{\text{ref}}/2 \quad -V_{\text{ref}}/4 \quad -V_{\text{ref}} \quad +V_{\text{ref}} \\
\end{align*}
\]
Operational Amplifiers

First stage is a telescopic cascode:
- Large DC gain:
  - Short–channel devices are OK
  - Low Parasitics
- 2 cascode nodes available for compensation:
  - Split Compensation Capacitors
give more Gain–Bandwidth or Phase–Margin

Two Common–Mode–Feedback loops:
- Good stability
- Outer loop is a SC circuit due to linearity requirements.

Main Specs:
- Slew rate: 166 V/μs
- Gain–Bandwidth: 200 MHz
1.5-Bit, Flash, sub-ADC

- No charge pumping. Low Power

- Sensitive to charge injection from switches, but:
  - Charge injection generate offsets
  - Offsets are removed through digital correction
Comparator

Low-gain Preamplifier
- Isolates input from kick-back noise
- Fast settling

Full-Swing Latch
- Fast regeneration. No metastability
- Rail-to-rail output

Clocked output
- Avoids non-CMOS levels

Circuit Diagram:

- Vi+, Vi-, Vbn
- M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11
- VDD, CLK, /CLK
- Out+, Out-
1.5–Bit sub–DAC

- High impedance output during phase 1. This saves 2 series–switches in the S&H circuit
- High linearity thanks to wire–crossing inversion
Digital Delay and Correction Circuit

Analog Pipeline

1. stage d1
   - p1 d0
   - p2 d1

2. stage d1
   - p1 d0
   - p2 d1

3. stage d1
   - p1 d0
   - p2 d1

4. stage d1
   - p1 d0
   - p2 d1

5. stage d1
   - p1 d0
   - p2 d1

6. stage d1
   - p1 d0
   - p2 d1

7. stage d1
   - p1 d0
   - p2 d1

8. stage d1
   - p1 d0
   - p2 d1

9. stage d1
   - p1 d0
   - p2 d1

(no amps)

- p1
- p2

D1 D2 D3 D4 D5 D6 D7 D8 D9
System–level Simulation

Single INL run

Monte–Carlo

Effects simulated:

- Capacitor mismatch  
- Finite opamp gain  
- Comparator offset  
- Digital correction logic.
Transistor–level Simulation (Spectre)

- Simulated from extracted circuit
- Distortion $< -60$ dB
- Power: 11.5 mW
  - Analog: 9.75 mW
  - Digital: 1.75 mW

Effects not included:
- Mismatch
- Circuit noise
Area: 1500 x 880 $\mu m^2$, including pads.
Measurements
Measured Nonlinearity Graphs

- Code density measurement with sinusoidal input.
Frequency-domain measurements

- Single and two-tone tests

- Continuous time and sampled sinusoids.
EVM measurements with real OFDM signals

- 54-Mbit/s OFDM signal (IEEE 802.11a/g). 10 MHz carrier.

- Agilent’s EVM test equipment & software.
Performance summary

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<table>
<thead>
<tr>
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<tbody>
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<td>10 bits</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>40 MHz</td>
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<td><strong>Power consumption</strong></td>
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<td>ADC: 11.7 mW</td>
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<td>( (C_L \approx 4.5 \text{ pF}) )</td>
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<td>Chip Area (w. pads)</td>
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<td>(wo. pads)</td>
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<td>Nonlinearity (max)</td>
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Operational Amplifiers

Inner CMFB Circuit

- Continuous-time
- Diff. pair + level shifter
- Small differential-input range

Outer CMFB Circuit

- Discrete-time
- Highly linear. Large input range
- Two circuits operate on alternate clock phases
# Performance summary

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<td>57.6 dB @ 1 MHz</td>
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<tr>
<td></td>
<td>57.8 dB @ 19.3 MHz†</td>
</tr>
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<td>59.0 dB @ 19.3 MHz††</td>
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Notes:

† Sampled input.

†† Sampled input and static INL correction.
OFDM modulation

⇒ Large number of subcarriers per channel.

⇒ Orthogonality = No interference bw. subcarriers.

\[
\int_0^{T_s} A_i \cos(\omega_i t + \varphi_i) \times A_j \cos(\omega_j t + \varphi_j) dt = 0
\]

⇒ OFDM modulation and demodulation are done via Fast Fourier Transforms (FFT).
OFDM (standard IEEE 802.11a/g)

- 64 sub-carriers, but
  - No DC carrier (f=0 Hz)
  - No carriers close to adjacent channels
- 54 used subcarriers.
- 48 carriers for data.
- Subcarrier modulation: QAM
- QAM constellations:
  - 64 (54 mb/s), 16 or 4 points.