Low Power Nyquist-Rate ADCs

10 bit, 40 Ms/s, pipeline ADC design.

2.5 V, 0.25 μm CMOS.

J. Arias
Global ADC architecture:

1.5 bits pipeline stage.
Modifications to previous design

 '-') Lower supply voltage: No enough room for a single cascode stage.

 '-') New opamps are two-stages. This gives more DC gain and output swing, but stability demands the use of compensation capacitors.

 '-') Comparators need a new design to accommodate the new input range.

 '-') Switches are fully CMOS transmission gates.
Opamps:

 ⇒ Specs:

✔ Slew-rate high enough to charge the load capacitances in 1/4 of sampling period. 

\( SR = 4V_{swing}f_s = 166V/\mu s \)

✔ Enough Unit-Gain Bandwidth to allow settling to \( 2^{-N} \) relative error in 1/4 of sampling period. 

\( GB \approx 10f_s = 200MHz \)

✔ DC gain well over \( 2^N \) to get good ADC linearity. (Gain>5000)

✔ Must be stable with a feedback factor about 1/2 (gain=2).

✔ Total opamp noise below quantization noise.
First stage is a telescopic cascode:
- Large DC gain:
  - Shorter channel devices.
  - Low Parasitics
- 2 cascode nodes available for compensation:
  - Split Compensation Capacitors gives more Gain–Bandwidth or Phase–Margin

Two Common–Mode–Feedback loops:
- Good stability
- Outer loop is a SC circuit due to linearity requirements.

Main Specs:
- Slew rate: 166 V/μs
- Gain–Bandwidth: 200 MHz
Opamp noise (simulation)

⇒ Small, N-channel, input devices can generate large $1/f$ noise, but the total noise integral is dominated by thermal noise due to the big bandwidth.

⇒ $1/f$ noise corner below 100 KHz.

⇒ Total integrated input noise (BW=200MHz) about $200\mu V$ rms. (15 dB below quantization noise)
- Continuous-Time CMFB possible because the output voltage swing of first stage is small.

- The circuit is a combination of source followers and level-shifter. It is a small load for the first stage.

- Small devices generate somewhat large noise, but this noise is mainly a common-mode signal.
- Two Switched Capacitor sets working on alternate clock phases.

- Highly linear. Linearity is needed because of the high output voltage swing.

- Output stage can drive large capacitors. CMFB circuit does not load the opamp significantly.
Switches

⇒ Rail-to-rail signals demands a fully complementary switch.

⇒ Low ON resistance required when charging large capacitors. (\( R_{ON} < 2K\Omega \) for 800fF capacitors).

⇒ Switch resistance varies with temperature and process. Worst case scenario must be taken into account.

⇒ Biggest switch: 7/0.28 \( \mu m \) (P-channel), 2.6/0.26 (N-channel). \( R_{ON} \) always below 1\( K\Omega \). Switches are scaled depending on load capacitance. Minimum size switch resistance: 26 \( K\Omega \).
Flash ADCs:

- Thanks to digital correction these ADCs do not need to be very accurate.

- 100pF level-shifting capacitors. These capacitors always remain charged.
- Regenerative comparator: Low gain preamp + Full swing latch.

- Fast regeneration (<1ns typ.): small chances of metastability.
High impedance output during phase 1. This saves 2 series-switches in the S&H circuit.

Switch size depends on pipeline position.
Stage scaling

<table>
<thead>
<tr>
<th>Stage</th>
<th>Cap. load (fF)</th>
<th>Scale factor</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1200</td>
<td>1</td>
<td>Reference design</td>
</tr>
<tr>
<td>2</td>
<td>400</td>
<td>1/3</td>
<td>-</td>
</tr>
<tr>
<td>3-8</td>
<td>300</td>
<td>1/4</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>-</td>
<td>-</td>
<td>Flash ADC only</td>
</tr>
</tbody>
</table>

⇒ Things scaled:

- Opamp currents, transistors and capacitors.
- Sampling capacitors.
- S&H switches and DAC switches.
S&H capacitor layout

First Stage layout

Other stages

Dummy capacitors used as power supply decoupling.
Digital delay & correction logic
Clock tree

clk input

125

2pF

(40 MHz)

1

Toggle

FF

2 phase
gen.

p1

p2

Global Clock Bus

(20 MHz)

Local

Clock

Bus

Pipeline stage

p1

/p1

p2

/p2

Digital delay network
Clock divider & 2-phase generator
Pin drivers

Vdddrv
(2.5 or 3.3 V)

Pin out
24/0.32 (10pF load max)

input
(2.5 V)

0.64/0.28
1/0.32

(10pF load max)
Power supply isolation

Substrate

ANALOG

DIGITAL

PIN DRIVER

vdda!
vdd!
vdddrv
gnd!
gnda!
Reference Voltages

- Short settling time: Small R.
- Power drain: 2.5 mW
- Common–mode reference does not need to be very accurate:
  - Big resistor divider
  - External decoupling capacitor
Pads

gnda

vdd
vdda

vdddrv

vdda/vdddrv

analog/digital IO

gnd
ADC layout
Linearity Simulation

Simulation conditions:

- Fully extracted circuit with parasitic capacitances (~50000 extracted devices)
- Pads & Bonding wires:
  
  \[
  3\text{nH} \quad 1\Omega
  \]
### ADC performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
<td>40 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>9.99 bits (1023 codes)</td>
</tr>
<tr>
<td>Technology</td>
<td>0.25 $\mu$m CMOS</td>
</tr>
<tr>
<td>Metal Layers</td>
<td>4</td>
</tr>
<tr>
<td>Chip Area (with pads)</td>
<td>1275$\mu$m x 670$\mu$m (0.85 mm$^2$)</td>
</tr>
<tr>
<td>Pin Count</td>
<td>22</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>$3^{rd}$ Harmonic Distortion</td>
<td>$&lt; -60$dB</td>
</tr>
<tr>
<td>Data Latency</td>
<td>300 ns</td>
</tr>
</tbody>
</table>
## Power Bill

<table>
<thead>
<tr>
<th>Source</th>
<th>Type</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>vdda! (2.5V)</td>
<td>Analog</td>
<td>3.9</td>
<td>9.75</td>
</tr>
<tr>
<td>vdd! (2.5V)</td>
<td>Digital. Core</td>
<td>0.7</td>
<td>1.75</td>
</tr>
<tr>
<td>ADC (2.5V)</td>
<td>TOTAL</td>
<td>4.6</td>
<td>11.5</td>
</tr>
<tr>
<td>Vdddrv (3.3 V)</td>
<td>Digital. Pin drivers</td>
<td>3.47</td>
<td>11.45</td>
</tr>
<tr>
<td>Vdddrv (2.5V)</td>
<td>(see notes)</td>
<td>2.57</td>
<td>6.44</td>
</tr>
</tbody>
</table>

Notes:

- Load capacitance = 10 pF
- Random data modulated OFDM (no guard time), 10 MHz shifted spectrum, full scale input, assumed.
- Bit transition power from pin driver circuit simulation.
To Do

‣ Empty areas:
  - More decoupling capacitors.
  - More ground pads.

‣ Chip completion:
  - Antenna check OK.
  - General Fill Pattern: Help needed.

‣ Submission.

‣ Package selection.
Last modifications

⇒ Dummy capacitors.

✔ Both plates are now connected to ground in order to avoid Vdd noise coupling to signal lines.

⇒ Protection diodes in Vdd pads.

✔ Vdd pads now only include one reverse-biased diode to ground. Forward-biased diode strings are removed because they seem to be not needed.

⇒ Pad spacing increased to 150 μm.

⇒ No pads in chip corners

⇒ Two more analog Vdd and ground pads.

⇒ Big decoupling capacitor for analog power supply added.
More data from simulation.

⇒ Integral non-linearity: 0.38 LSB (nominal corner)

⇒ 20 Ms/s operation @ Iref = 5 $\mu$A (nominal Iref = 10 $\mu$A)

✔ ADC power: 7.125 mW.

✔ Non-linearity: 0.3 LSB

⇒ Chip area, with pads: 1500 x 880 $\mu m^2$