Design of a CMOS Fully Differential Switched-Opamp for SC Circuits at Very Low Power Supply Voltages

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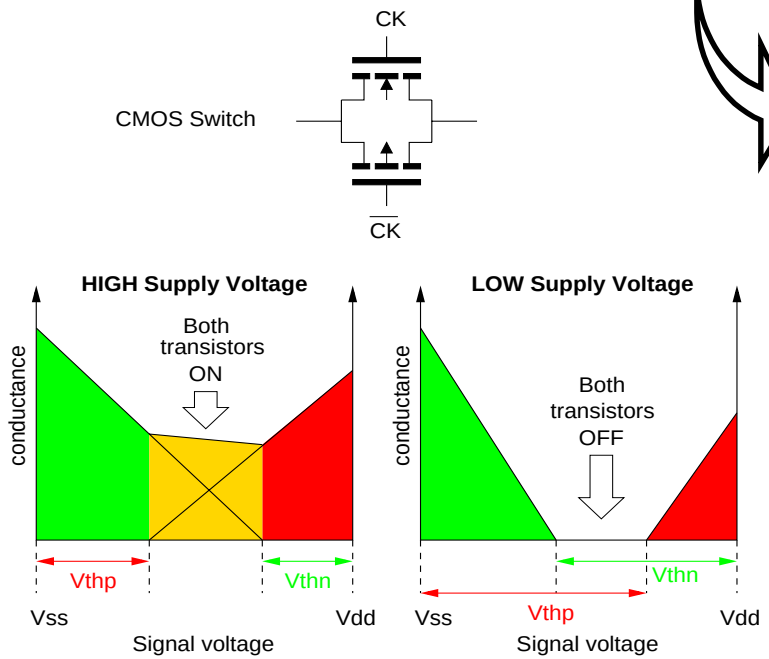
Outline

- Introduction
- Switched-Opamp Design
- Simulation Results
- Experimental Results
- Switched-Opamp Application
- Conclusions

Introduction: Very Low Power Supply Voltage

☆ **Interest towards low-voltage IC´s due to**
- ✓ **portable equipment**
- ✓ **technology scaling**

☆ **For low-cost integration, SC circuits are well-suited for CMOS technology**



SC Circuits at Very Low Voltages

The key problem !!!

Switches cannot pass rail–to–rail signals below a certain V_{DD} supply level

Introduction: Switched–Opamp Approach [Crols & Steyaert, 94]

Classical SC Integrator. **Two types of switches:**

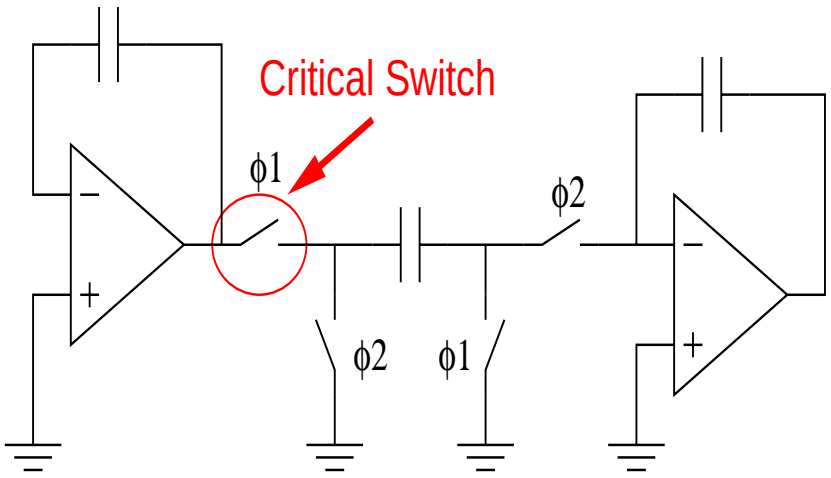
i) with one terminal connected to the reference level or

ii) connected to a signal source (critical switch)

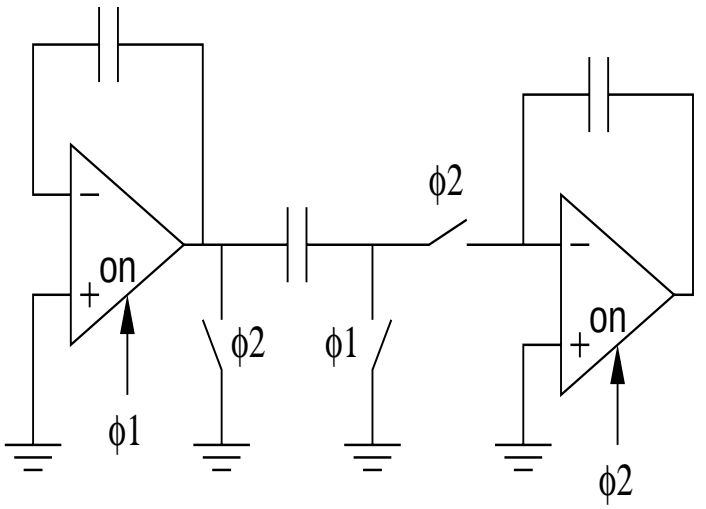
Switched-Opam Approach: **i) Critical switches are eliminated**

ii) Opams are ON/OFF

Typical SC integrator topology



Switched Opamp integrator topology



Objective: Switched-Opamp Design and Implementation

✖ Switched-Opamp for SC circuits

Target Specifications:

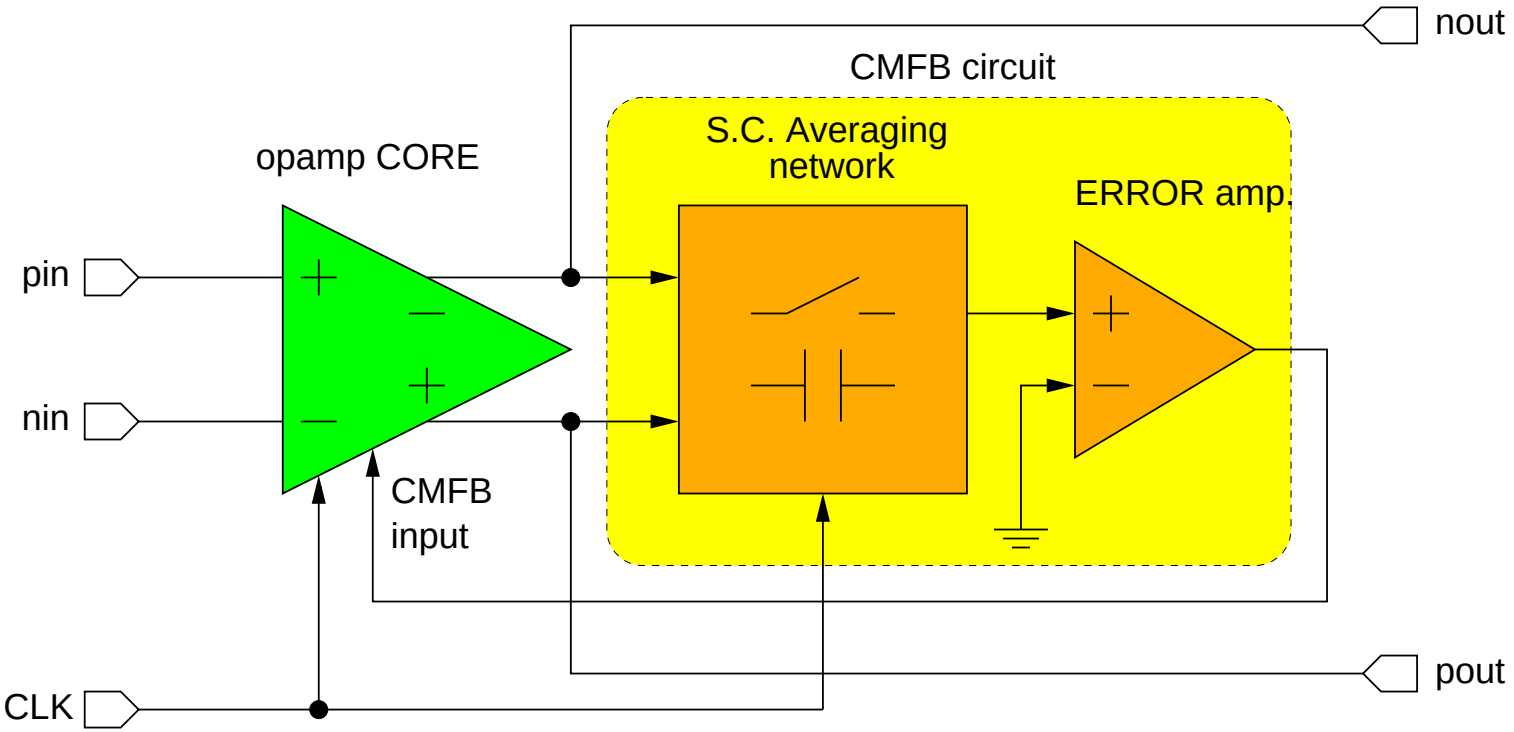
- ✓ **CMOS technology: 0.35 microns, 3.3V (V_{THN} = 0.5V, V_{THP} = - 0.65V)**
- ✓ **Supply voltage: 1V**
- ✓ **Sampling frequency: f_{clock} = 1 MHz**
- ✓ **Open-loop gain: higher than 70 dB**
- ✓ **Maximum load capacitance: 5 pF**
- ✓ **Unity-gain bandwidth: $f_u = 5 \times f_{clock}$ = 5 MHz (with 5 pF)**

Application:

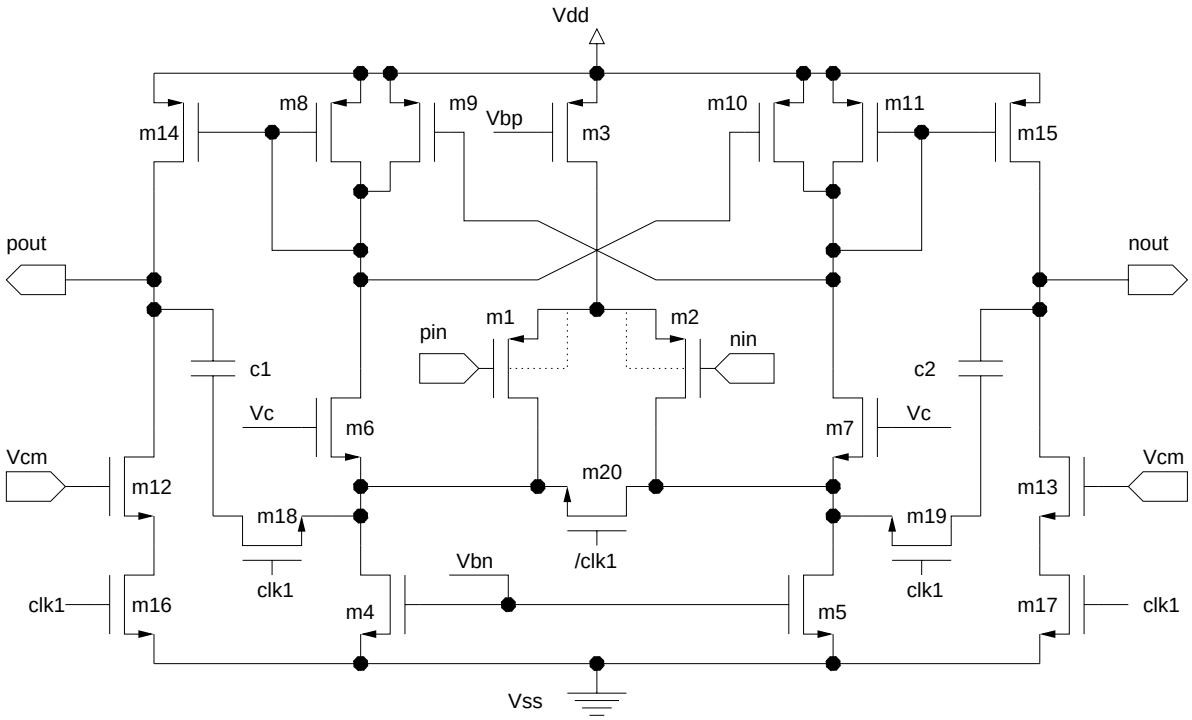
A bandpass filter using the Switched-Opamp for Radio Data System (RDS) was designed and implemented

Switched-Opamp Design: Funcional Blocks

- ✖ **Output voltage range from rail-to-rail**
- ✖ **Fully differential structure**
  (a CMFB circuit must be included)

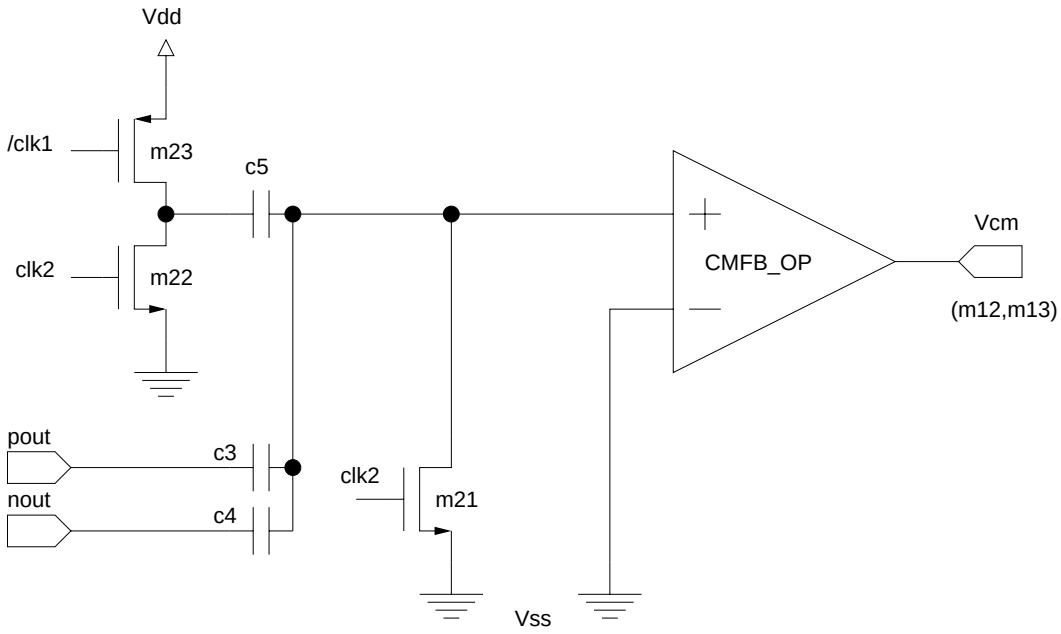


Switched-Opamp Design: Core Description [Waltari & Halonen, 98]



- ✓ **Two stage folded cascode topology with cascoded Miller compensation (C1 = C2 = 1 pF)**
- ✓ **Input stage: Cross-coupled loads ⇨ high CMRR**
- ✓ **Switches:**
  - **m16 and m17: only output stage is OFF and outputs are connected to V_{DD}**
  - **m18 and m19: no discharge of Cc during OFF**
  - **m20: no saturation of the input stage during OFF**
- ✓ **Minimum power supply: $V_{DD} - V_{SS} = V_{THP} + 3\,V_{DSSAT}$ ⇨ $V_{DD,\,MIN} = 1V$**

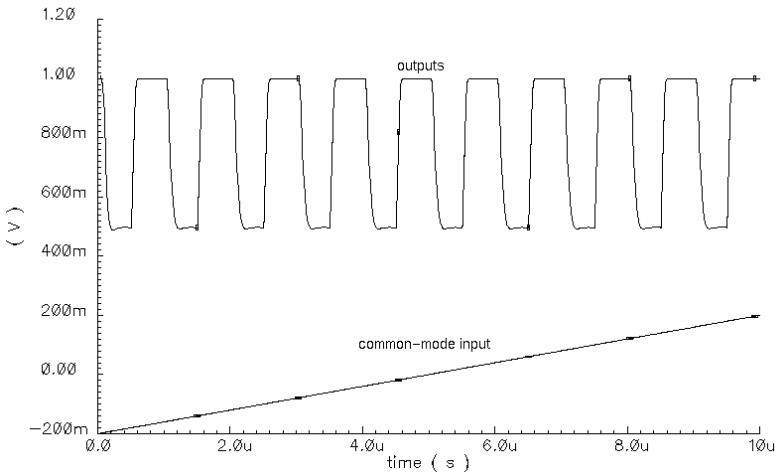
Switched-Opamp Design: CMFB Description

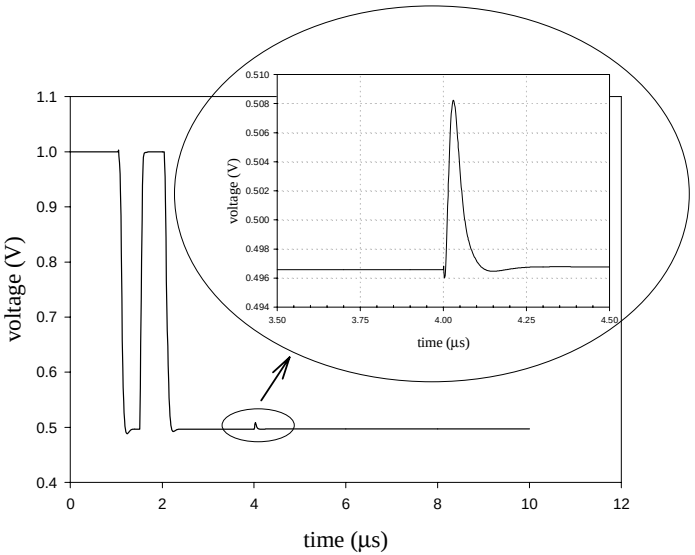


- ✓ **CMFB consists of:**
  switched-capacitors (C3 = C4 = C5 = 0.25 pF), and an single-ended error amplifier

- ✓ **CMFB is applied to the core output stage**

Simulation Results: Common-Mode Response

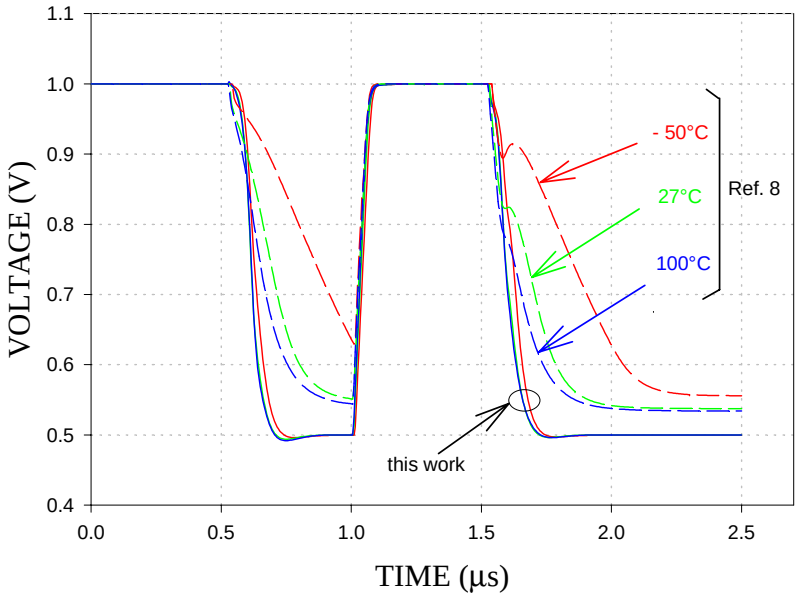




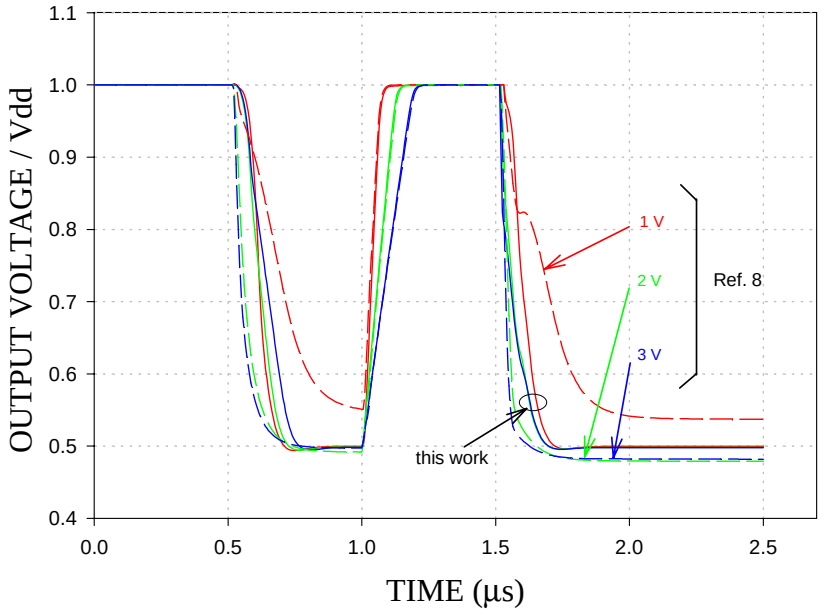
- ✓ **High CMRR**
- ✓ **Common-Mode Settling Time: 200 ns**

The common-mode output is stabilized in just one clock cycle

Simulation Results: Common-Mode Response for Different Temperatures and Power Supply Voltages



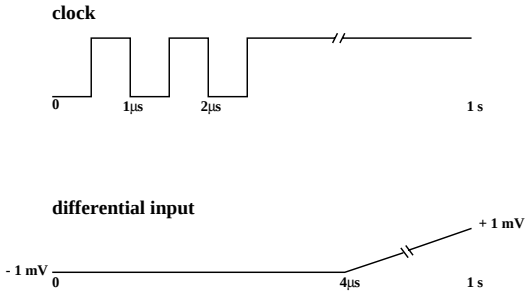
V_{DD} = 1V, and T = -50°C, 27°C, 100°C

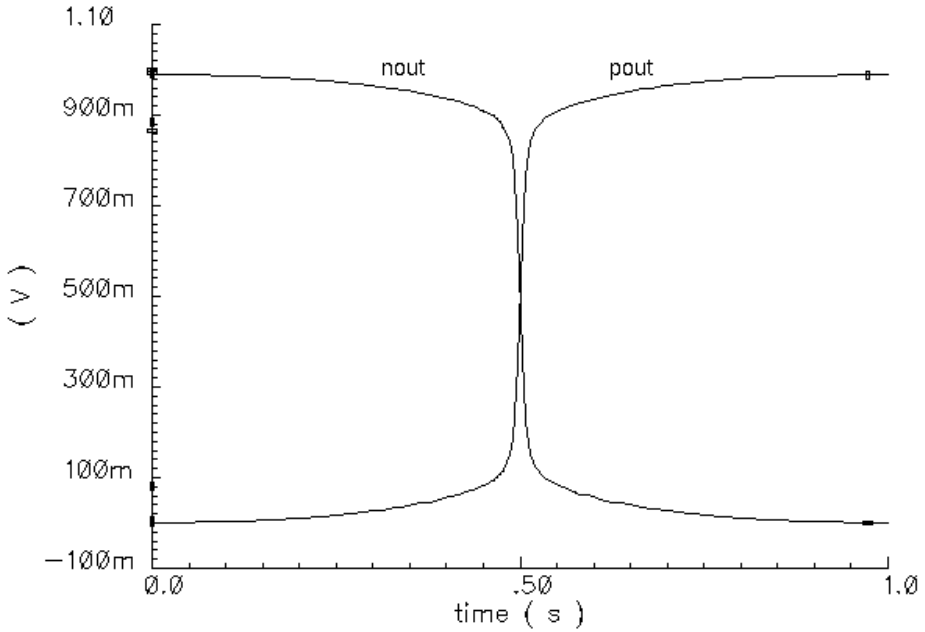


T = 27°C, and V_{DD} = 1V, 2V, 3V

- ✓ **High accuracy**
- ✓ **Low sensitivity to T and V_{DD}**
- ✓ **No excessive area penalty**

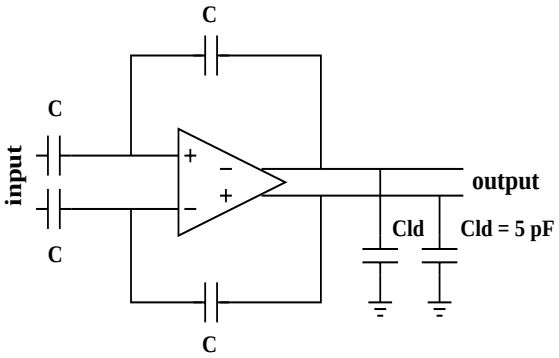
Simulation Results: DC Differential Transfer Characteristic

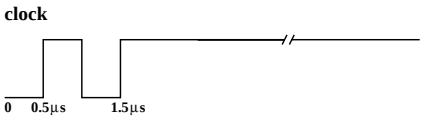


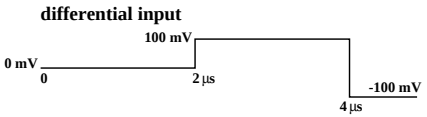


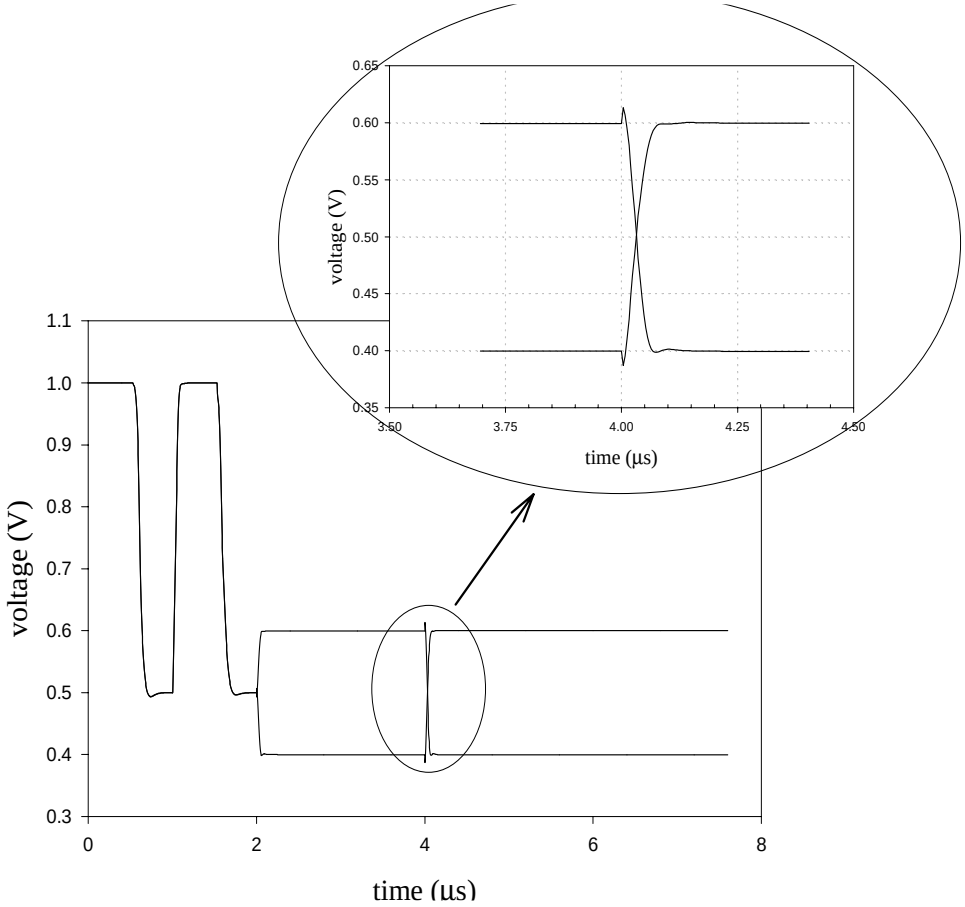
- ✓ **DC gain: 86 dB**
- ✓ **Rail-to-rail output range: 100 mV - 900 mV**

Simulation Results: Step Response and Settling





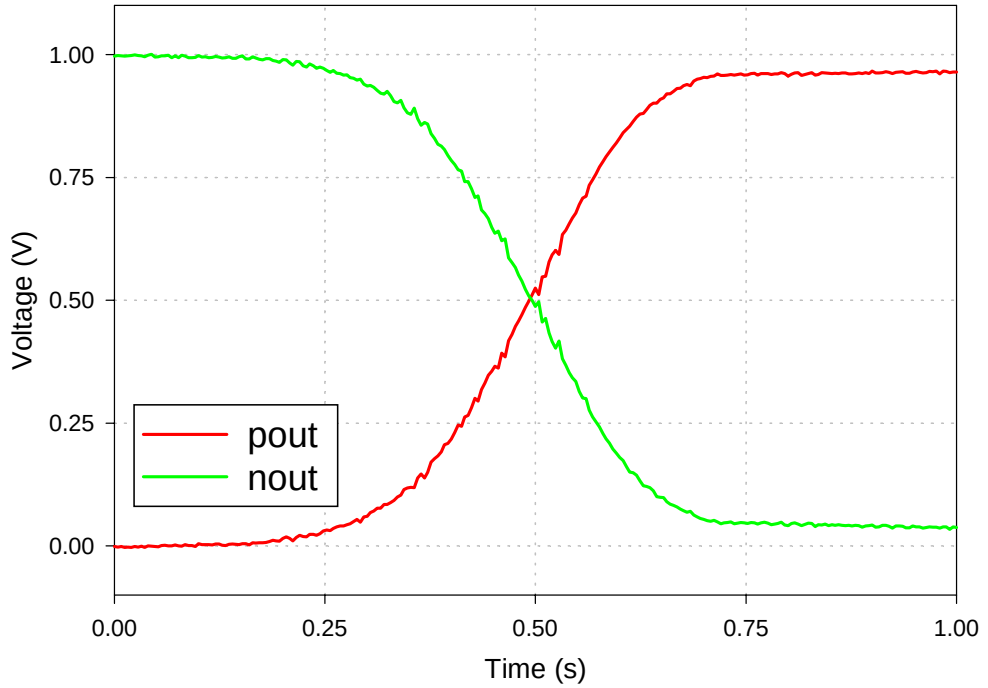




✓ **Small Signal Step Response.** Settling Time = 60 ns

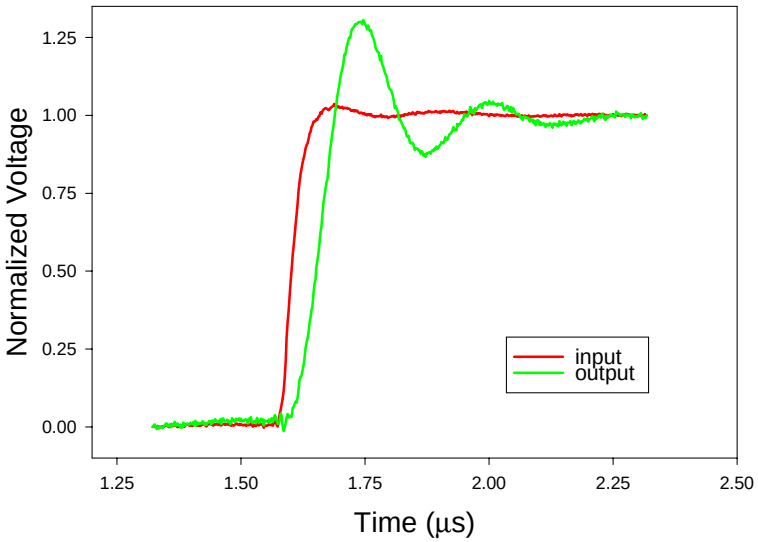
✓ **Large Signal Step Response.** Slew Rate = 4.7 V/µs

Experimental Results: DC Differential Transfer Characteristic



- ✓ **DC Gain: 76 dB**
- ✓ **Rail-to-Rail Output Range: 140 mV- 860 mV**
- ✓ **Offset: 1 mV**

Experimental Results: Settling and Switching Behaviour

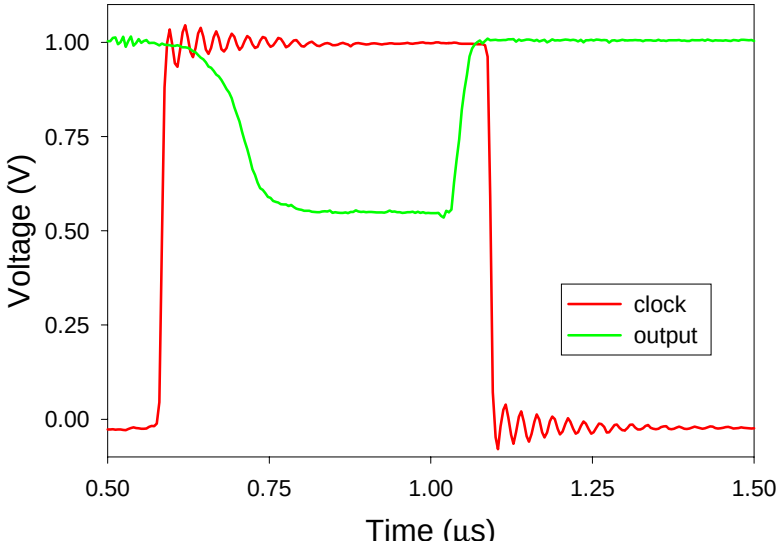


✓**Small Signal Step Response.**

For V_{step} = 100 mV, Settling Time = 200 ns

✓ **Large Signal Step Response.**

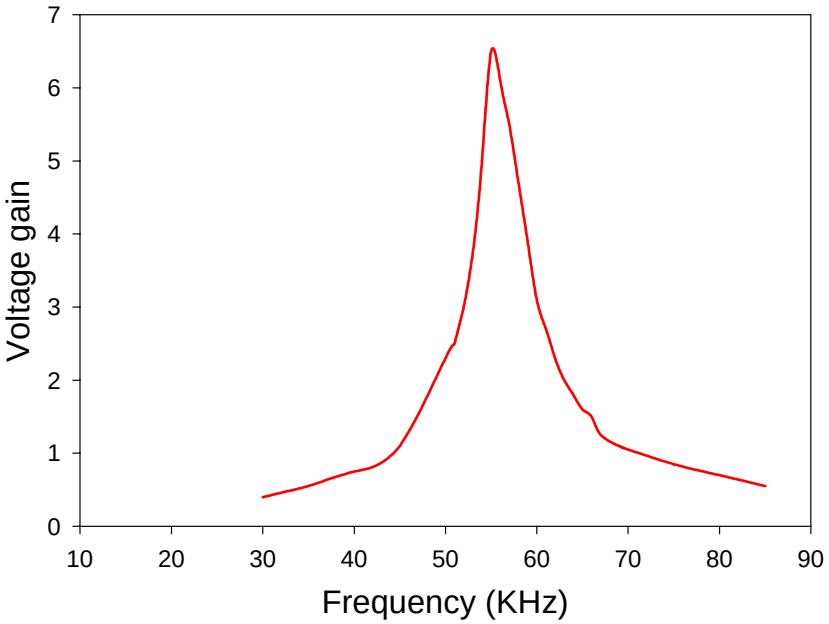
For V_{step} = 700 mV, Slew Rate = 4.3 V/µs

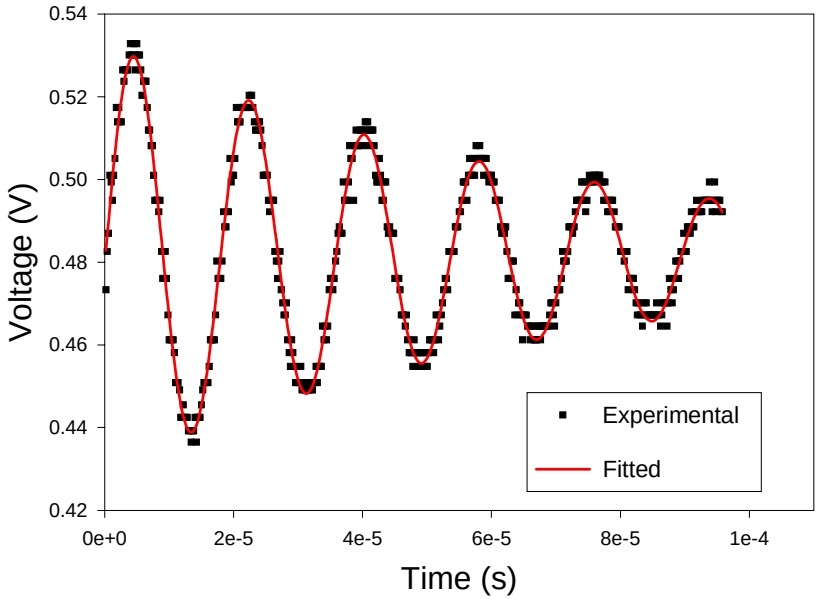


Switching Time of the Opamp: 250 ns

Switched-Opamp Application: Bandpass Filter for RDS

✖ Filter was based on an E-type Fleischer-Laker topology





From frequency response and step-induced transient:

central frequency, f_0: 57 KHz
quality factor, Q: 12.5
voltage gain: 6.5

Conclusions

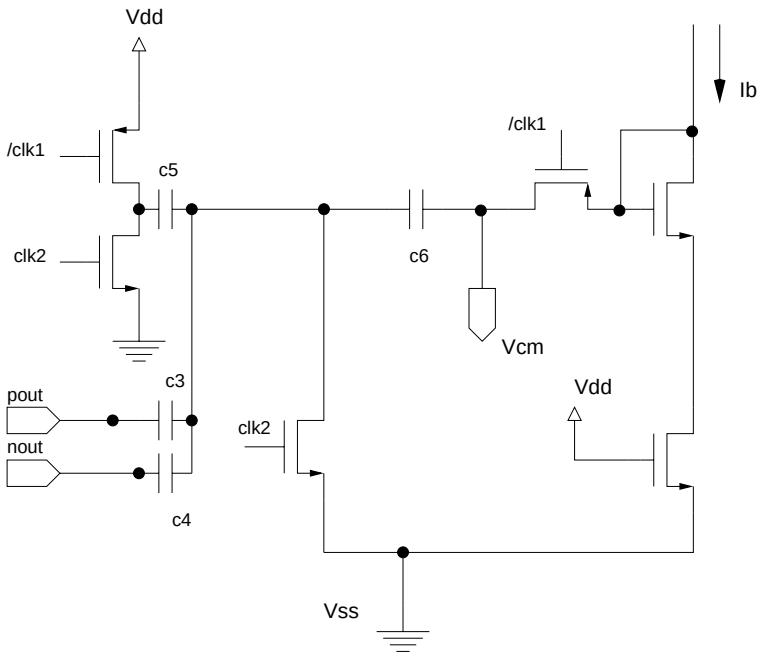
- A **Switched-Opamp** for very low voltage (V_{DD} = 1V) SC circuits was **designed and implemented** in 0.35 microns CMOS technology.

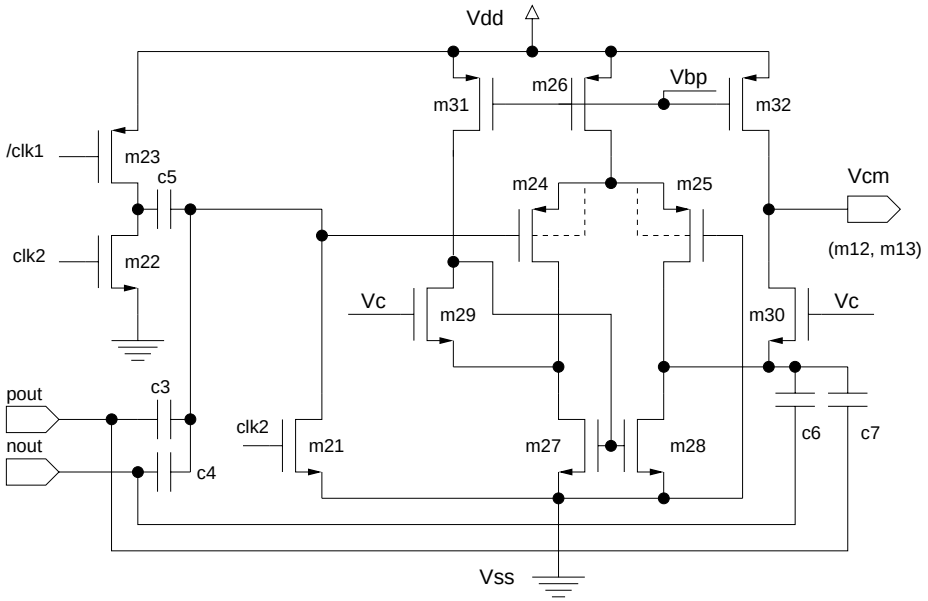
- Some of its **features** are:
  - ✓ **Core**
    - » fully differential topology, and
    - » rail-to-rail output.
  - ✓ **CMFB**
    - » consists of **switched-capacitors and an error amplifier**,
    - » only operates on the output stage, and
    - » high accuracy and low sensitivity to T and V_{DD}

- **Simulated and experimental results** are shown.

- **Application:** a **bandpass filter** based on the Switched-Opamp was designed and implemented.

Switched Opamp Design: CMFB Circuits Comparison





CMFB circuit proposed by Waltari et al.

Ib is a replica of the current in the core output stage.

CMFB_OP circuit used in this work:

- ✓ **two stage folded cascoded topology with cascoded Miller compensation**
- ✓ **the CMFB_OP output stage is the same as the core output stage**

Opamp Performance Summary

Parameter	Simulated Value	Experimental Value
Power supply	1 V	1 V
Power consumption	90 µW @ 1V	93 µW @ 1V
Unity gain bandwidth	7.9 MHz	4.7 MHz
Open loop gain	86 dB	76 dB
SR up	4.6 V/µs	4.2 V/µs
SR down	5 V/µs	4.5 V/µs
Phase margin	62^0	-
Active Cell area	0.02 mm^2	0.02 mm^2