Continuous-time, multibit, complex $\Delta \Sigma$ ADC

320 Ms/s, 16x oversampling, 3-bit quantizer, 10-bit ENOB.

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Motivation

⇒ Why complex ΔΣ:

✔ Channel selection and image rejection are done in the digital domain by the decimation filter.

✔ Easy analog filtering. (good IQ imbalance, low power)

⇒ Why continuous-time (CT):

✔ Capable of operation at high sampling frequencies.

✔ Low power consumption.

✔ Implicit anti-aliasing property.

⇒ Why multibit:

✔ Good SNR for low oversampling ratios. (16)

✔ Good stability.
Drawbacks

⇒ ΔΣ ADCs:

× ΔΣ ADCs requires high sampling rates (oversampling ≥ 16, typical)

× A digital filter/decimator is needed (several K gates).

× ΔΣ ADCs consume more power than Nyquist-rate ADCs. (But the total power bill can be lower)

⇒ CT ΔΣ modulators:

× Involves DT to CT transformations (NTF) ⇒ Tedious mathematics & controllability issues.

× CT modulators are more sensitive to clock jitter.

⇒ Multibit ΔΣ modulators:

× Sensitive to DAC nonlinearity. Dynamic element matching (scrambler) needed.
IEEE 802.11a/g, low-IF, receiver with Nyquist-rate ADC

Complex BPF (1×):

$BW = 20 \text{ MHz}, f_{IF} = 10 \text{ MHz}$

7-pole Chebyshev filter

(Vladimir)

Nyquist ADC (1×):

$BW = 20 \text{ MHz}, SNDR = 55 \text{ dB}$

10-bit pipelined ADC

(Jesús)
IEEE 802.11a/g, low-IF, receiver with $\Delta \Sigma$ ADC

Complex BPF:
$BW = 20 \text{ MHz}, f_{IF} = 10 \text{ MHz}$

3-pole Butterworth filter

Complex CT $\Delta \Sigma$ ADC:
$BW = 20 \text{ MHz}, SNDR = 55 \text{ dB}$

2nd-order 3-bit 16 $\times$ oversampled

(Vladimir) Proposed architecture (Peter/Vladimir/Jesús)
Modulator architecture (Real DSM)

Starting modulator

After amplitude equalization

- Second-order NTF
- Optimized zero: +3dB SNR
- 3-bit ADC and DAC
- RZ DAC: less sensitive to:
  - ADC metastability
  - Clock jitter
Gm–C Implementation (Real DSM, Single-ended)
Multibit DACs: Overcoming nonlinearity using dynamic element matching
DWA logic (scrambler)

- 8-bit Rotator
- Thermometer to binary
- DSM output
- from ADC to DACs
- Reg. Reg.clk clk
- RZ es esp esn
- clk

Σ

Reg.
Thermal noise

Noise simulation parameters:

GM1: 1000 $\mu$A/V  C1: 5.165 pF
GM2: 200 $\mu$A/V  C2: 0.376 pF
GM3: 15 $\mu$A/V

$I_{b1}$: 714 $\mu$A  $I_{dac1}$: 95.4 $\mu$A
$I_{b2}$: 147 $\mu$A  $I_{dac2}$: 20.1 $\mu$A

Performance loss: 2 dB SNR
Real DSM. Detailed schematic

- **Ibias1**: 714 µA
- **GM1**: 1000 µS
- **DAC1**: 8 x 95.4 µA
- **C1**: 5.16 pF
- **GM2**: 200 µS
- **DAC2**: 8 x 20.1 µA
- **C2**: 0.37 pF
- **Ibias2**: 147 µA
- **GM3**: 15 µS
- **CMFB**
- **7-level ADC**
- **Scrambler logic**

**Analog input** to **DSM output**
Circuit Elements: Transconductors

- Large dynamic range
- Unipolar output
- External tuning
- Vladimir’s patent (2001)
Circuit Elements: Transconductor’s nonlinear $G_m$

\[ G_m(x) = G_m(0) \frac{d}{dx} \left\{ \tanh \left( x + \frac{0.82}{3} x^3 + \frac{2.14}{5} x^5 - \frac{0.60}{7} x^7 \right) \right\} \]
Circuit Elements: Small Transconductors (GM3)

- Pseudodifferential: poor common mode rejection
- Good linearity
- Low accuracy: Gm depends on Vcas and Cm(Vin)
- Low power efficiency
Channel resistance is not simulated unless "nqsmod=1" is specified on every capacitor.

Big capacitors must be split into parallel, small, capacitors to improve their Q.
Circuit Elements: ADC

![Diagram of ADC circuit with labeled components.](Diagram.png)
Circuit Elements: ADC biasing
Circuit Elements: ADC’s comparators

Comparator & Latch

Vi+
Vi−

Vdd

ck

/dck

out

NC

Signal Timming

clk
dck

internal nodes

track.
regen.
track.
transp.
latched

out

sample N−1

sample N

sampling window
Circuit Elements: Current-mode DACs

Current–mode DACs

Current cell

Signal timing

Io+
Io−
esn0 esp0 esn1 esp1 esn7 esp7
Vcas
Vbias
Vref
esp
esn
ck
esp
esn
Circuit Elements: CMFB
Real DSM results (spectre simulation with extracted blocks)

(2048 samples)

SNR = 61 dB
SNDR = 57 dB
Complex DSM schematic

Two real modulators

Ampl. (dB)
Freq. (MHz)
Complex DSM schematic

Two real modulators

Complex modulator
Cross-coupled transconductor switching
Clock distribution

- Clock source
- External capacitor (~10pF)
- Clock pin
- 15 kΩ
- 10 fF

Components:
- ADC
- SCR
- SCR
Pin drivers
Circuit Layout (2.5-V, 0.25-$\mu$m CMOS, $1480 \times 880 \, \mu m^2$)
Simulated results (extracted circuit)

- Full extracted circuit with parasitic capacitances
- Two-tone test show no intermodulation products
- SNR: 55 dB (+3dB dual tone)
- Total power ~25 mW
Before chip submission

=> Chip completion.

✔ Antenna check
  o Is it removed from Cadence?

✔ Fill patterns
  o What are they for?
  o Are they really needed?

=> Other issues....
Setup for measurement