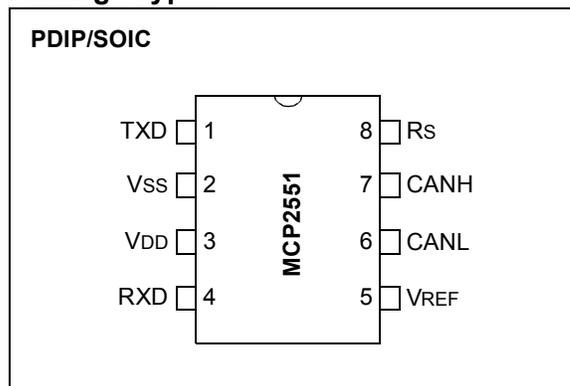


High Speed CAN Transceiver

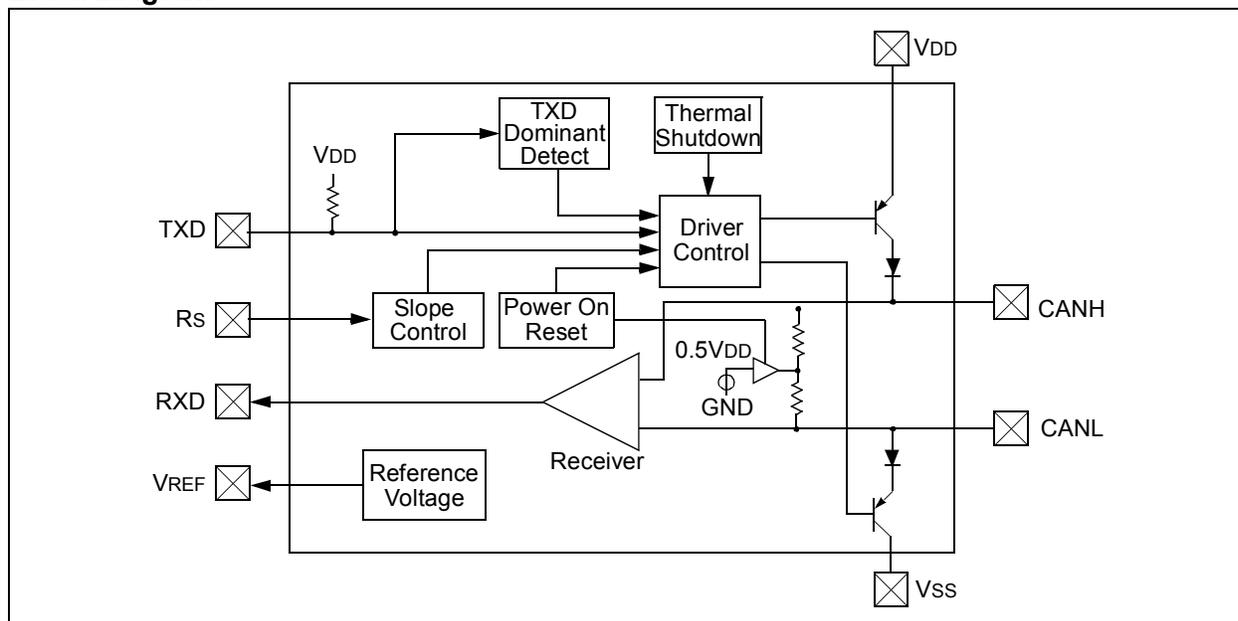
Features

- Supports 1 Mb/s operation
- Implements ISO 11898 standard physical layer requirements
- Suitable for 12 V and 24 V systems
- Externally controlled slope for reduced RFI emissions
- Detection of ground fault (permanent dominant) on TXD input
- Power-on reset and voltage brown-out protection
- An unpowered node or brown-out event will not disturb the CAN bus
- Low current standby operation
- Protection against damage due to short circuit conditions (positive or negative battery voltage)
- Protection against high voltage transients
- Automatic thermal shutdown protection
- Up to 112 nodes can be connected
- High noise immunity due to differential bus implementation
- Temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Extended (E): -40°C to +125°C

Package Types



Block Diagram



MCP2551

NOTES:

1.0 DEVICE OVERVIEW

The MCP2551 is a high speed CAN fault tolerant device that serves as the interface between a CAN protocol controller and the physical bus. The MCP2551 provides differential transmit and receive capability for the CAN protocol controller and is fully compatible with the ISO 11898 standard, including 24 V requirements. It will operate at speeds of up to 1 Mb/s.

Typically, each node in a CAN system must have a device to convert the digital signals generated by a CAN controller to signals suitable for transmission over the bus cabling (differential output). It also provides a buffer between the CAN controller and the high voltage spikes that can be generated on the CAN bus by outside sources (EMI, ESD, electrical transients, etc.).

1.1 Transmitter Function

The CAN bus has two states: Dominant and Recessive. A dominant state occurs when the differential voltage between CANH and CANL is greater than a defined voltage (e.g., 1.2 V). A recessive state occurs when the differential voltage is less than a defined voltage (typically 0 V). The dominant and recessive states correspond to the low and high state of the TXD input pin, respectively. However, a dominant state initiated by another CAN node will override a recessive state on the CAN bus.

1.1.1 MAXIMUM NUMBER OF NODES

The MCP2551 CAN outputs will drive a minimum load of 45 Ω , allowing a maximum of 112 nodes to be connected (given a minimum differential input resistance of 20 k Ω and a nominal termination resistor value of 120 Ω).

1.2 Receiver Function

The RXD output pin reflects the differential bus voltage between CANH and CANL. The low and high states of the RXD output pin correspond to the Dominant and Recessive states of the CAN bus, respectively.

1.3 Internal Protection

CANH and CANL are protected against battery short circuits and electrical transients that can occur on the CAN bus. This feature prevents destruction of the transmitter output stage during such a fault condition.

The device is further protected from excessive current loading by thermal shutdown circuitry that disables the output drivers when the junction temperature exceeds a nominal limit of 165°C. All other parts of the chip remain operational and the chip temperature is lowered due to the decreased power dissipation in the transmitter outputs. This protection is essential to protect against bus line short-circuit induced damage.

1.4 Operating Modes

The Rs pin allows three modes of operation to be selected:

- High Speed
- Slope Control
- Standby

These modes are summarized in Table 1-1.

When in high speed or slope control mode, the drivers for the CANH and CANL signals are internally regulated to provide controlled symmetry in order to minimize EMI emissions.

In addition, the slope of the signal transitions on CANH and CANL can be controlled with a resistor connected from pin 8 (Rs) to ground, with the slope proportional to the current output at Rs, further reducing EMI emissions.

1.4.1 HIGH SPEED

The high speed mode is selected by connecting the Rs pin to Vss. In this mode, the transmitter output drivers have fast output rise and fall times to support high-speed CAN bus rates.

1.4.2 SLOPE CONTROL

Slope control mode further reduces EMI by limiting the rise and fall times of CANH and CANL. The slope, or slew rate (SR), is controlled by connecting an external resistor (R_{EXT}) between Rs and Vol (usually ground). The slope is proportional to the current output at the Rs pin. Since the current is primarily determined by the slope-control resistance value R_{EXT}, a certain slew rate is achieved by applying a respective resistance. Figure 1-1 illustrates typical slew rate values as a function of the slope-control resistance value.

1.4.3 STANDBY MODE

The device may be placed in standby or "sleep" mode by applying a high level to Rs. In sleep mode, the transmitter is switched off and the receiver operates at a lower current. The receive pin on the controller side (RXD) is still functional but will operate at a slower rate. The attached microcontroller can monitor RXD for CAN bus activity and place the transceiver into normal operation via the Rs pin (at higher bus rates the first CAN message may be lost).

MCP2551

TABLE 1-1: MODES OF OPERATION

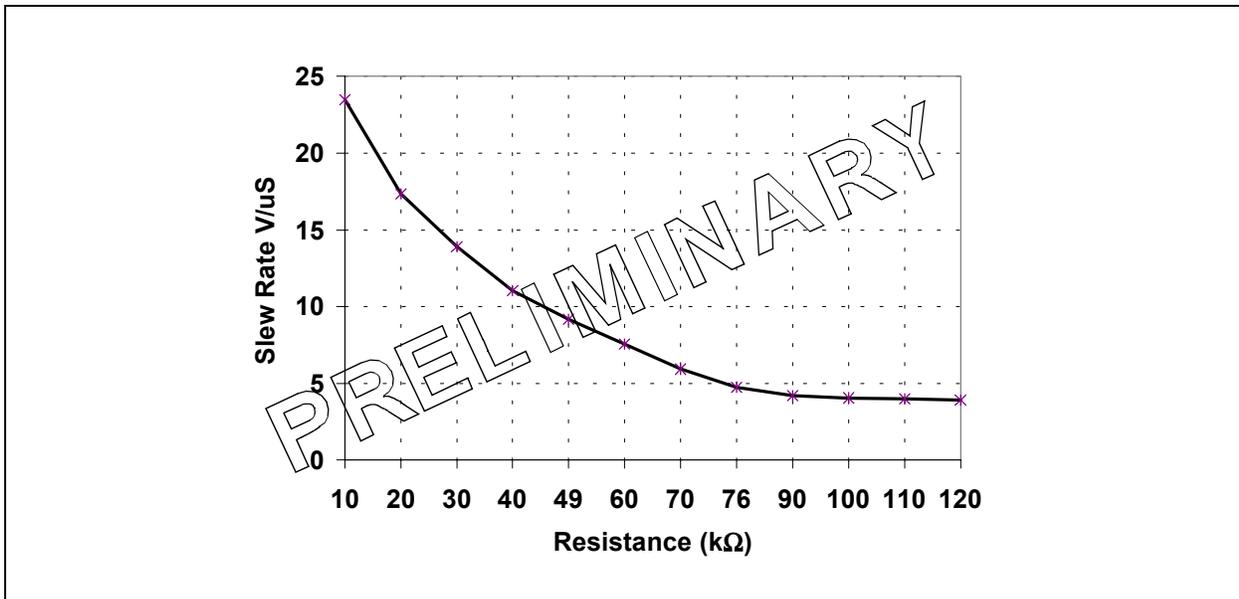
Mode	Current at R_s Pin	Resulting Voltage at R_s Pin
Standby	$-I_{RS} < 10 \mu A$	$V_{RS} > 0.75V_{DD}$
Slope Control	$10 \mu A < -I_{RS} < 200 \mu A$	$0.4V_{DD} < V_{RS} < 0.6V_{DD}$
High Speed	$-I_{RS} < 610 \mu A$	$0 < V_{RS} < 0.3V_{DD}$

TABLE 1-2: TRANSCEIVER TRUTH TABLE

VDD	VRS	TXD	CANH	CANL	Bus State ⁽¹⁾	RxD ⁽¹⁾
$4.5 V \leq V_{DD} \leq 5.5 V$	$V_{RS} < 0.75V_{DD}$	0	HIGH	LOW	Dominant	0
		1 or floating	Not Driven	Not Driven	Recessive	1
	$V_{RS} > 0.75V_{DD}$	X	Not Driven	Not Driven	Recessive	1
$V_{POR} < V_{DD} < 4.5 V$ (See Note 3)	$V_{RS} < 0.75V_{DD}$	0	HIGH	LOW	Dominant	0
		1 or floating	Not Driven	Not Driven	Recessive	1
	$V_{RS} > 0.75V_{DD}$	X	Not Driven	Not Driven	Recessive	1
$0 < V_{DD} < V_{POR}$	X	X	Not Driven/ No Load	Not Driven/ No Load	High Impedance	X

- Note 1:** If another bus node is transmitting a dominant bit on the CAN bus, then RXD is a logic 0.
Note 2: X = "don't care".
Note 3: Device drivers will function, although outputs are not guaranteed to meet ISO-11898 specification.

FIGURE 1-1: SLEW RATE VS. SLOPE CONTROL RESISTANCE VALUE



1.5 TXD Permanent Dominant Detection

If the MCP2551 detects an extended low state on the TXD input, it will disable the CANH and CANL output drivers in order to prevent the corruption of data on the CAN bus. The drivers are disabled if TXD is low for more than 1.25 ms (minimum). This implies a maximum bit time of 62.5 μ s or minimum bus rate of 16 kb/s (allowing a maximum 20 consecutive transmitted dominant bits during a multiple bit error and error frame scenario). The drivers remain disabled as long as TXD remains low. A rising edge on TXD will reset the timer logic and enable the CANH and CANL output drivers.

1.6 Power-on Reset

When the device is powered on, CANH and CANL remain in a high impedance state until VDD reaches the voltage level VPORH. In addition, CANH and CANL will remain in a high impedance state if TXD is low when VDD reaches VPORH. CANH and CANL will become active only after TXD is asserted high. Once powered on, CANH and CANL will enter a high impedance state if the voltage level at VDD falls below VPORL, providing voltage brown-out protection during normal operation.

1.7 Pin Descriptions

The 8-pin pinout is listed in Table 1-3.

TABLE 1-3: MCP2551 PINOUT

Pin Number	Pin Name	Pin Function
1	TXD	Transmit Data Input
2	VSS	Ground
3	VDD	Supply Voltage
4	RXD	Receive Data Output
5	VREF	Reference Output Voltage
6	CANL	CAN Low Level Voltage I/O
7	CANH	CAN High Level Voltage I/O
8	Rs	Slope Control Input

1.7.1 TRANSMITTER DATA INPUT (TXD)

TXD is a TTL compatible input pin. The data on this pin is driven out on the CANH and CANL differential output pins. It is usually connected to the transmitter data output of the CAN controller device. When TXD is low, CANH and CANL are in the dominant state. When TXD is high, CANH and CANL are in the recessive state (provided that another CAN node is not driving the CAN bus with a dominant state). TXD has an internal pull-up resistor (nominal 25 k Ω to VDD.)

1.7.2 GROUND SUPPLY (VSS)

Ground supply pin.

1.7.3 SUPPLY VOLTAGE (VDD)

Positive supply voltage pin.

1.7.4 RECEIVER DATA OUTPUT (RXD)

RXD is a TTL compatible output that drives high or low depending upon the differential signals on the CANH and CANL pins and is usually connected to the receiver data input of the CAN controller device. RXD is high when the CAN bus is recessive and low in the dominant state.

1.7.5 REFERENCE VOLTAGE (VREF)

Reference Voltage Output. (Defined as VDD/2).

1.7.6 CAN LOW (CANL)

The CANL output drives the low side of the CAN differential bus. This pin is also tied internally to the receive input comparator.

1.7.7 CAN HIGH (CANH)

The CANH output drives the high side of the CAN differential bus. This pin is also tied internally to the receive input comparator.

1.7.8 SLOPE RESISTOR INPUT (Rs)

The Rs pin is used to select High Speed, Slope Control, or Standby modes via an external biasing resistor.

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2.0 ELECTRICAL CHARACTERISTICS

2.1 Terms and Definitions

A number of terms are defined in ISO 11898 that are used to describe the electrical characteristics of a CAN transceiver device. These terms and definitions are summarized in this section.

2.1.1 BUS VOLTAGE

V_{CANL} and V_{CANH} , denoting the voltages of the bus line wires, CANL and CANH, relative to ground of each individual CAN node.

2.1.2 COMMON MODE BUS VOLTAGE RANGE

Boundary voltage levels of V_{CANL} and V_{CANH} with respect to ground, for which proper operation will occur, if up to the maximum number of CAN nodes are connected to the bus.

2.1.3 DIFFERENTIAL INTERNAL CAPACITANCE, C_{DIFF} (OF A CAN NODE)

Capacitance seen between CANL and CANH during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.4 DIFFERENTIAL INTERNAL RESISTANCE, R_{DIFF} (OF A CAN NODE)

Resistance seen between CANL and CANH during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.5 DIFFERENTIAL VOLTAGE, V_{DIFF} (OF CAN BUS)

Differential voltage of the two-wire CAN bus, value $V_{DIFF} = V_{CANH} - V_{CANL}$.

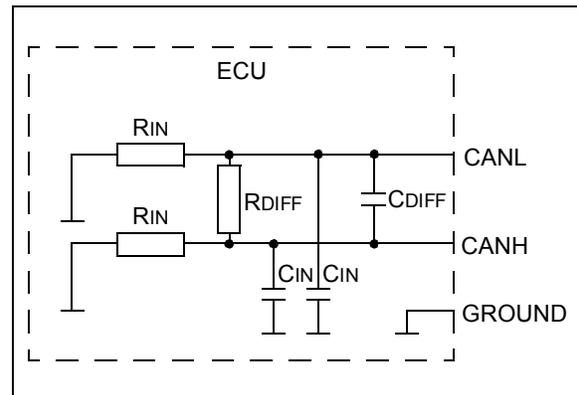
2.1.6 INTERNAL CAPACITANCE, C_{IN} (OF A CAN NODE)

Capacitance seen between CANL (or CANH) and ground during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

2.1.7 INTERNAL RESISTANCE, R_{IN} (OF A CAN NODE)

Resistance which is seen between CANL (or CANH) and ground during the recessive state when the CAN node is disconnected from the bus (see Figure 2-1).

FIGURE 2-1: PHYSICAL LAYER DEFINITIONS



Absolute Maximum Ratings†

VDD.....	7.0 V
DC Voltage at TXD, RXD, VREF and VS.....	-0.3 V to VDD+0.3 V
DC Voltage at CANH, CANL (Note 1).....	-42 V to +42 V
Transient Voltage on Pins 6 and 7 (Note 2).....	-250 V to +250 V
Storage temperature	-55°C to +150°C
Operating ambient temperature	-40°C to +125°C
Virtual Junction Temperature, TVJ (Note 3)	-40°C to +150°C
Soldering temperature of leads (10 seconds)	+300°C
ESD protection on all pins (Note 4)	4 kV

Note 1: Short circuit applied when TXD is high and when TXD is low.

2: In accordance with ISO 7637.

3: In accordance with IEC 60747-1.

4: Classification A: Human Body Model.

† NOTICE: Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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2.2 DC Characteristics

DC Specifications			Electrical Characteristics:			
			Industrial (I): $T_{AMB} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{DD} = 4.5\text{ V}$ to 5.5 V			
			Extended (E): $T_{AMB} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ $V_{DD} = 4.5\text{ V}$ to 5.5 V			
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
Supply:						
D1	IDD	Supply Current	—	75	mA	Dominant; $V_{TXD} = 0.8\text{ V}$; V_{DD}
D2			—	10	mA	Recessive; $V_{TXD} = +2\text{ V}$; $R_s = 47\text{ k}\Omega$
D3			—	295	μA	$-40^{\circ}\text{C} \leq T_{AMB} \leq +85^{\circ}\text{C}$, Standby; Note 2
			—	450	μA	$-40^{\circ}\text{C} \leq T_{AMB} \leq +125^{\circ}\text{C}$, Standby; Note 2
D4	VPORH	High level of the power-on reset comparator	3.8	4.3	V	CANH, CANL outputs are active when $V_{DD} > V_{PORH}$
D5	VPORL	Low level of the power-on reset comparator	3.4	4.0	V	CANH, CANL outputs are not active when $V_{DD} < V_{PORL}$
D6	VPORD	Hysteresis of power-on reset comparator	0.3	0.8	V	Note 1
Bus line (CANH; CANL) transmitter:						
D7	$V_{CANH(r)}; V_{CANL(r)}$	CANH, CANL Recessive bus voltage	2.0	3.0	V	$V_{TXD} = V_{DD}$; no load.
D8	$I_{O(CANH)(reces)}$ $I_{O(CANL)(reces)}$	Recessive output current	-2	+2	mA	$-2\text{ V} < V(CAHL, CANH) < +7\text{ V}$, $0\text{ V} < V_{DD} < 5.5\text{ V}$
D9			-10	+10	mA	$-5\text{ V} < V(CANL, CANH) < +40\text{ V}$, $0\text{ V} < V_{DD} < 5.5\text{ V}$
D10	$V_{O(CANH)}$	CANH dominant output voltage	2.75	4.5	V	$V_{TXD} = 0.8\text{ V}$
D11	$V_{O(CANL)}$	CANL dominant output voltage	0.5	2.25	V	$V_{TXD} = 0.8\text{ V}$
D12	$V_{DIFF(r)(o)}$	Recessive differential output voltage	-500	+50	mV	$V_{TXD} = 2\text{ V}$; no load
D13	$V_{DIFF(d)(o)}$	Dominant differential output voltage	1.5	3.0	V	$V_{TXD} = 0.8\text{ V}$; $40\ \Omega < R_L < 60\ \Omega$ Note 2
D14	$I_{O(SC)(CANH)}$	CANH short circuit output current	—	-200	mA	$V_{CANH} = -5\text{ V}$
D15			—	-100 (typical)	mA	$V_{CANH} = -40\text{ V}, +40\text{ V}$. Note 1
D16	$I_{O(SC)(CANL)}$	CANL short circuit output current	—	200	mA	$V_{CANL} = -40\text{ V}, +40\text{ V}$. Note 1
Bus line (CANH; CANL) receiver: [TXD = 2V; pins 6 and 7 externally driven]						
D17	$V_{DIFF(r)(i)}$	Recessive differential input voltage	-1.0	+0.5	V	$-2\text{ V} < V(CANL, CANH) < +7\text{ V}$. Note 3
			-1.0	+0.4	V	$-12\text{ V} < V(CANL, CANH) < +12\text{ V}$. Note 3
D18	$V_{DIFF(d)(i)}$	Dominant differential input voltage	0.9	5.0	V	$-2\text{ V} < V(CANL, CANH) < +7\text{ V}$. Note 3
			1.0	5.0	V	$-12\text{ V} < V(CANL, CANH) < +12\text{ V}$. Note 3
D19	$V_{DIFF(h)(i)}$	Differential input hysteresis	100	200	mV	see Figure 2-4. Note 1
D20	RIN	CANH, CANL common mode input resistance	5	50	k Ω	
D21	RIN(d)	Deviation between CANH and CANL common mode input resistance	-3	+3	%	$V_{CANH} = V_{CANL}$

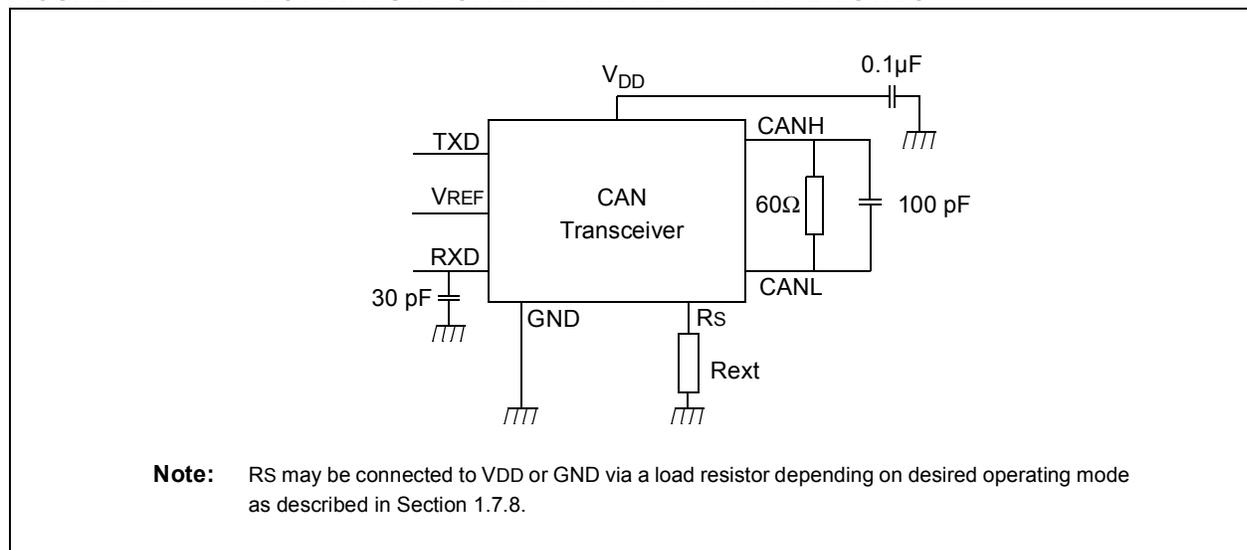
- Note 1:** This parameter is periodically sampled and not 100% tested.
Note 2: $I_{TXD} = I_{RXD} = I_{VREF} = 0\text{ mA}$; $0\text{ V} < V_{CANL} < V_{DD}$; $0\text{ V} < V_{CANH} < V_{DD}$; $V_{RS} = V_{DD}$.
Note 3: This is valid for the receiver in all modes, high-speed, slope control and standby..

2.2 DC Characteristics (Continued)

DC Specifications (Continued)			Electrical Characteristics:			
			Industrial (I): $T_{AMB} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{DD} = 4.5\text{ V}$ to 5.5 V			
			Extended (E): $T_{AMB} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ $V_{DD} = 4.5\text{ V}$ to 5.5 V			
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
Bus line (CANH; CANL) receiver: [TXD = 2V; pins 6 and 7 externally driven]						
D22	R_{DIFF}	Differential input resistance	20	100	$k\Omega$	
D24	I_{LI}	CANH, CANL input leakage current	—	250	μA	$V_{DD} < V_{POR}$; $V_{CANH} = V_{CANL} = +5\text{ V}$
Transmitter data input (TXD):						
D25	V_{IH}	High level input voltage	2.0	—	V	Output recessive
D26	V_{IL}	Low level input voltage	—	+0.8	V	Output dominant
D27	I_{IH}	High level input current	-30	+30	μA	$V_{TXD} = V_{DD}$
D28	I_{IL}	Low level input current	-100	-400	μA	$V_{TXD} = 0\text{ V}$
Receiver data output (RXD):						
D31	I_{OH}	High level output current	8	—	mA	$V_{RXD} = 0.7V_{DD}$ min
D32	I_{OL}	Low level output current	8	—	mA	$V_{RXD} = 0.8\text{ V}$ max
Voltage reference output (VREF):						
D33	V_{REF}	Reference output voltage	$0.45V_{DD}$	$0.55V_{DD}$	V	$-50\ \mu\text{A} < I_{VREF} < 50\ \mu\text{A}$
Standby/Slope control (Rs pin):						
D34	V_{STB}	Input voltage for standby mode	$0.75V_{DD}$	—	V	
D35	I_{SLOPE}	Slope control mode current	-10	-200	μA	
D36	V_{SLOPE}	Slope control mode voltage	$0.4V_{DD}$	$0.6V_{DD}$	V	
Thermal Shutdown:						
D37	$T_{J(sd)}$	Shutdown junction temperature	155	180	$^{\circ}\text{C}$	Note 1
D38	$T_{J(h)}$	Shutdown temperature hysteresis	20	30	$^{\circ}\text{C}$	$-12\text{ V} < V(\text{CANL}, \text{CANH}) < +12\text{ V}$. Note 3

- Note 1:** This parameter is periodically sampled and not 100% tested.
Note 2: $I_{TXD} = I_{RXD} = I_{VREF} = 0\text{ mA}$; $0\text{ V} < V_{CANL} < V_{DD}$; $0\text{ V} < V_{CANH} < V_{DD}$; $V_{RS} = V_{DD}$.
Note 3: This is valid for the receiver in all modes, high-speed, slope control and standby..

FIGURE 2-2: TEST CIRCUIT FOR ELECTRICAL CHARACTERISTICS



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FIGURE 2-3: TEST CIRCUIT FOR AUTOMOTIVE TRANSIENTS

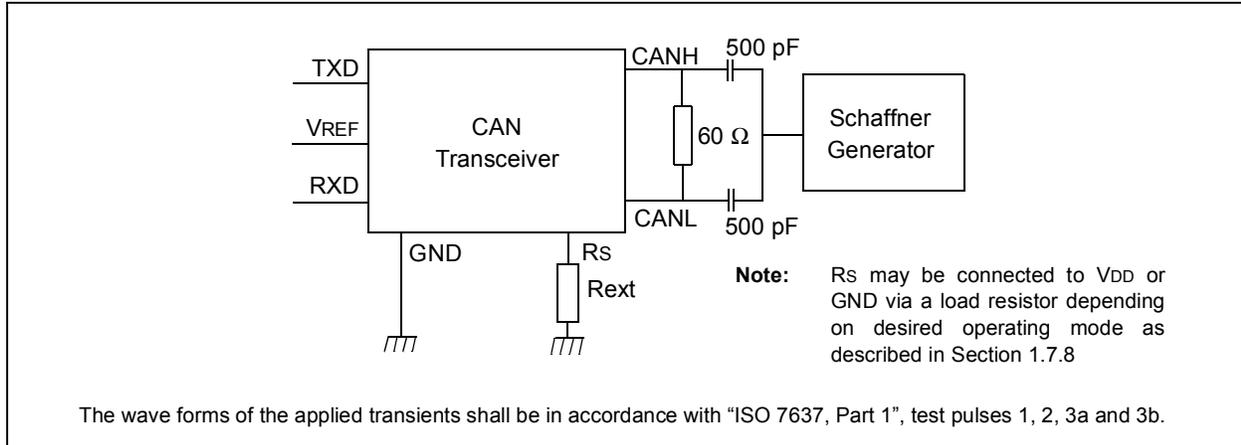
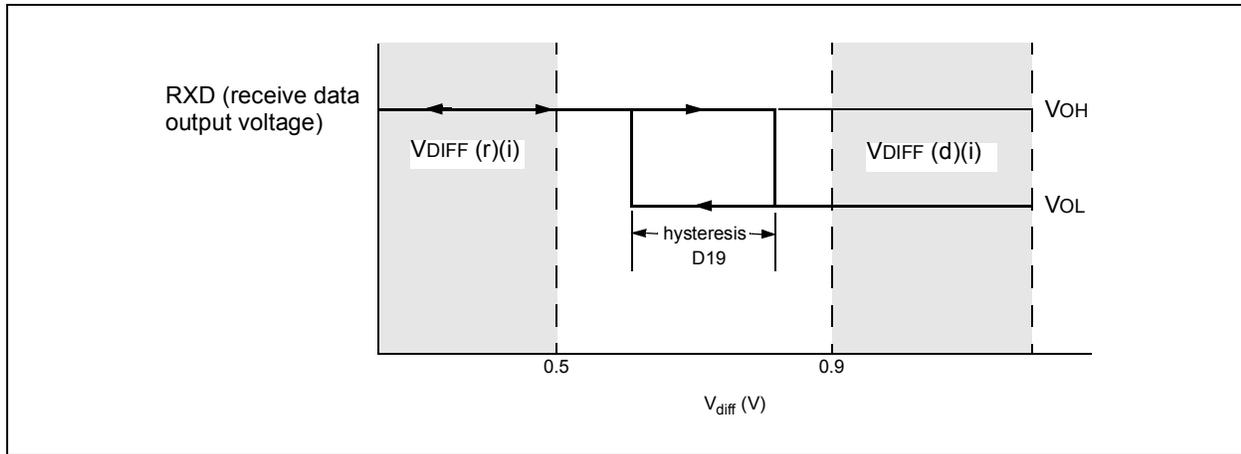


FIGURE 2-4: HYSTERESIS OF THE RECEIVER



2.3 AC Characteristics

AC Specifications			Electrical Characteristics: Industrial (I): T _{AMB} = -40°C to +85°C V _{DD} = 4.5 V to 5.5 V Extended (E): T _{AMB} = -40°C to +125°C V _{DD} = 4.5 V to 5.5 V			
Param No.	Sym	Characteristic	Min	Max	Units	Conditions
1	t _{BIT}	Bit time	1	62.5	μs	V _{RS} = 0 V
2	f _{BIT}	Bit frequency	16	1000	kHz	V _{RS} = 0 V
3	T _{txL2bus(d)}	Delay TXD to bus active	—	70	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0 V
4	T _{txH2bus(r)}	Delay TXD to bus inactive	—	125	ns	-40°C ≤ T _{AMB} ≤ +85°C, V _{RS} = 0 V
			—	170	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0 V
5	T _{txL2rx(d)}	Delay TXD to receive active	—	150	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0 V
			—	250	ns	-40°C ≤ T _{AMB} ≤ +125°C, R _S = 47 kΩ
6	T _{txH2rx(r)}	Delay TXD to receiver inactive	—	175	ns	-40°C ≤ T _{AMB} ≤ +85°C, V _{RS} = 0 V
			—	210	ns	-40°C ≤ T _{AMB} ≤ +85°C, R _S = 47 kΩ
			—	220	ns	-40°C ≤ T _{AMB} ≤ +125°C, V _{RS} = 0 V
			—	400	ns	-40°C ≤ T _{AMB} ≤ +125°C, R _S = 47 kΩ
7	SR	CANH, CANL slew rate	5.5	8.5	V/μs	Refer to Figure 1-1; R _S = 47 kΩ, Note 1
10	t _{WAKE}	Wake-up time from standby (R _S pin)	—	20	μs	see Figure 2-6
11	T _{busD2rx(s)}	Bus dominant to RXD Low (standby mode)	—	3	μs	V _{RS} = +4V; see Figure 2-7
12	C _{IN(CANH)}	CANH; CANL input capacitance	—	20 (typical)	pF	1 Mbit/s data rate; V _{TXD} = V _{DD} , Note 1
	C _{IN(CANL)}					
13	C _{DIFF}	Differential input capacitance	—	10 (typical)	pF	1 Mbit/s data rate Note 1
14	T _{txL2busZ}	TX Permanent Dominant Timer Disable Time	1.25	4	ms	
15	T _{txR2pdt(res)}	TX Permanent Dominant Timer Reset Time	—	1	μs	Rising edge on TXD while device is in permanent dominant state

Note 1: This parameter is periodically sampled and not 100% tested.

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2.4 Timing Diagrams and Specifications

FIGURE 2-5: TIMING DIAGRAM FOR AC CHARACTERISTICS

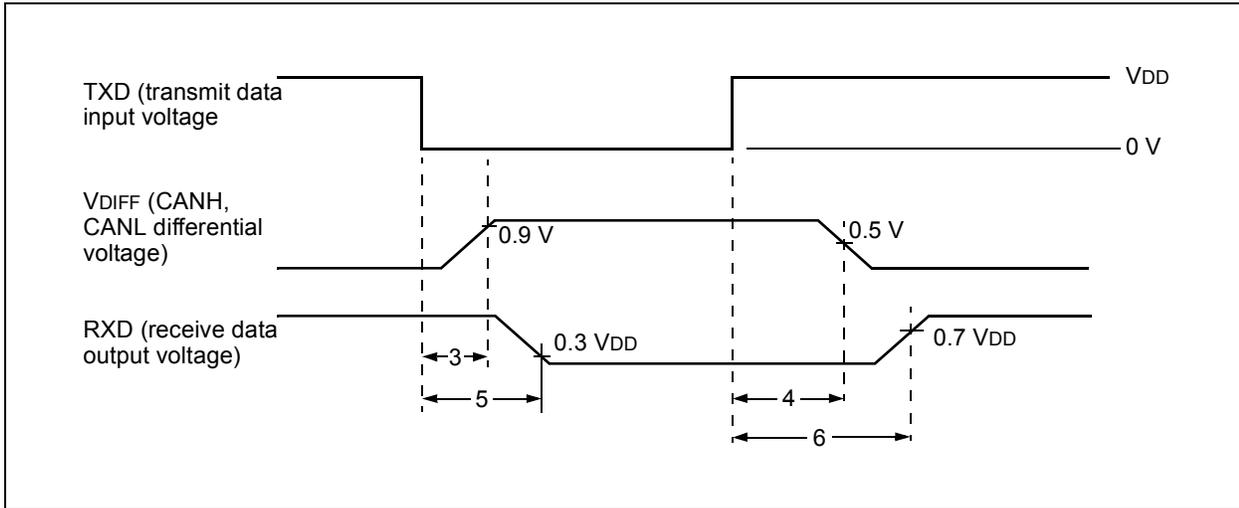


FIGURE 2-6: TIMING DIAGRAM FOR WAKEUP FROM STANDBY

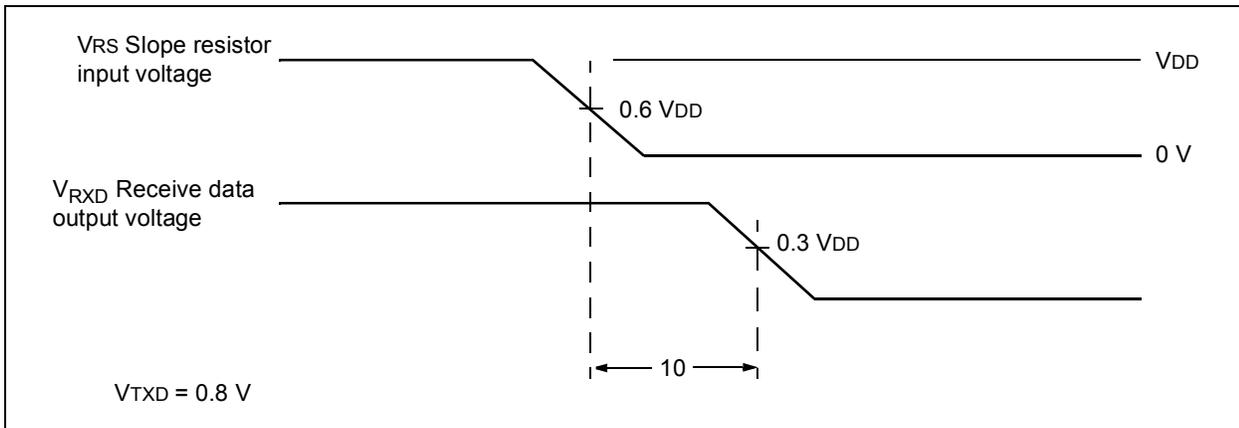
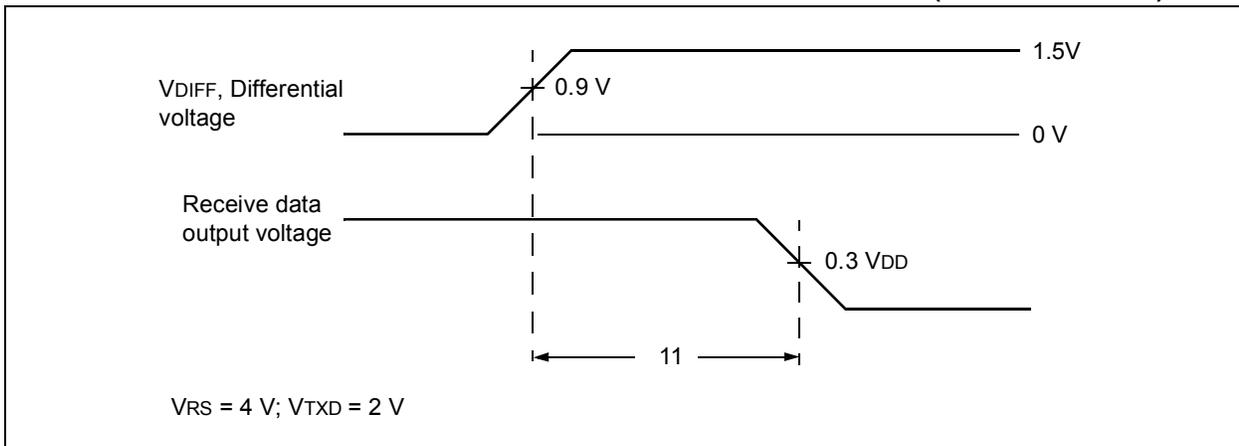


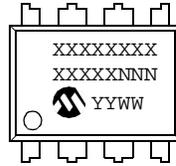
FIGURE 2-7: TIMING DIAGRAM FOR BUS DOMINANT TO RXD LOW (STANDBY MODE)



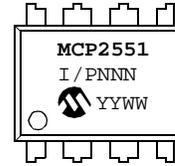
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

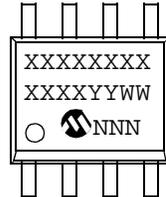
8-Lead PDIP (300 mil)



Example:



8-Lead SOIC (150 mil)



Example:

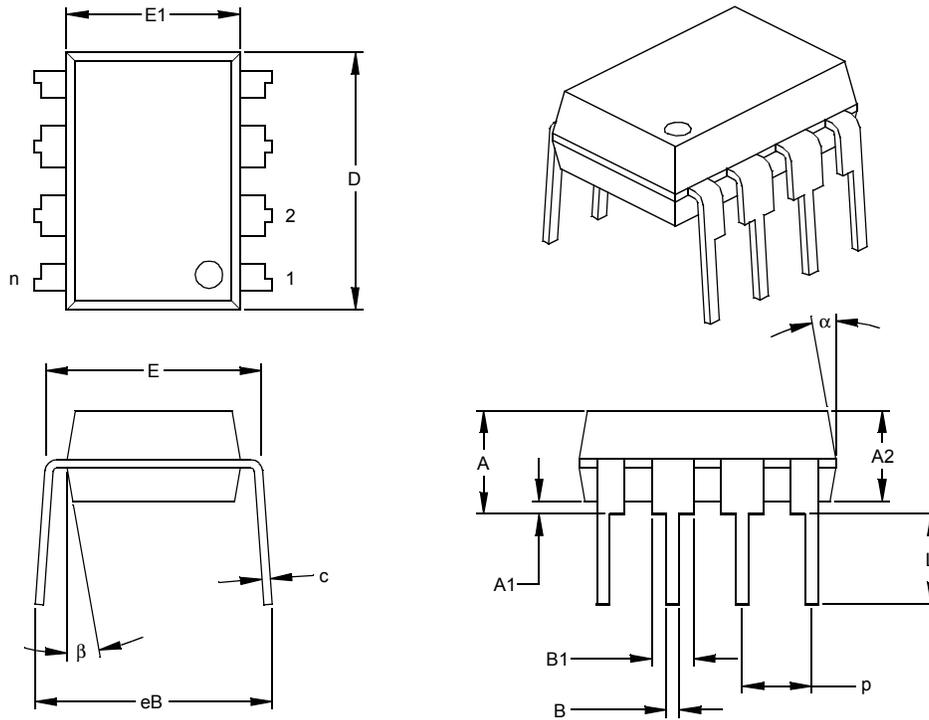


Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.	

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

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8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

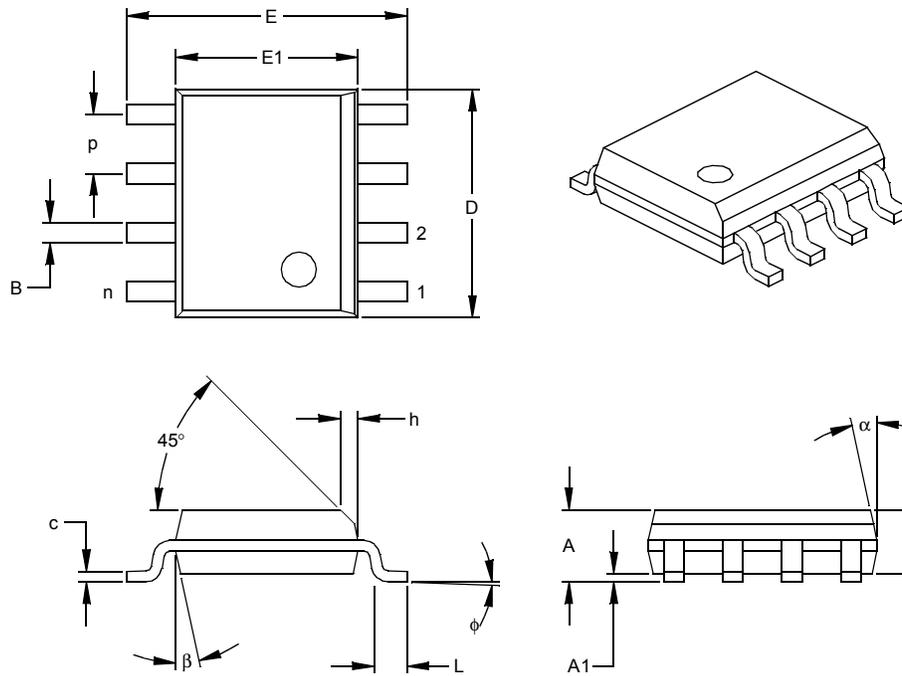
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

MCP2551

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Temperature Range:	I = -40°C to +85°C	
	E = -40°C to +125°C	
Package:	P = Plastic DIP (300 mil Body) 8-lead	
	SN = Plastic SOIC (150 mil Body) 8-lead	

Examples:

- MCP2551-I/P: Industrial temperature, PDIP package.
- MCP2551-E/P: Extended temperature, PDIP package.
- MCP2551-I/SN: Industrial temperature, SOIC package.
- MCP2551T-I/SN: Tape and Reel, Industrial Temperature, SOIC package.
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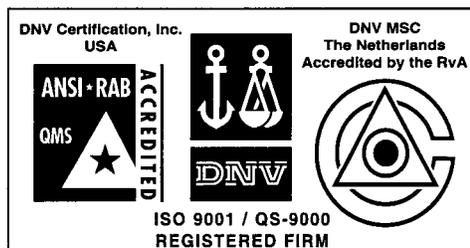
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New York

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Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology (Barbados) Inc.,
Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

Austria

Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

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