The information presented in this chapter is collected from the Microcontroller Architectural Overview, AT89C51, AT89LV51, AT89C52, AT89LV52, AT89C2051, and AT89C1051 data sheets of this book. The material has been selected and rearranged to form a quick and convenient reference for the programmers of Atmel's microcontroller family of devices. This guide pertains specifically to the AT89C51, AT89LV51, AT89C52, and AT89LV52.

Memory Organization

Program Memory

The AT89C Microcontroller has separate address spaces for program memory and data memory. The program memory can be up to 64K bytes long. The lower addresses may reside on-chip.

Figure 1 shows a map of the AT89C51 program memory, and Figure 2 shows a map of the AT89C52 program memory. The AT89C1051/2051 do not have off-board memory expansion.

Figure 1. AT89C51 Program Memory

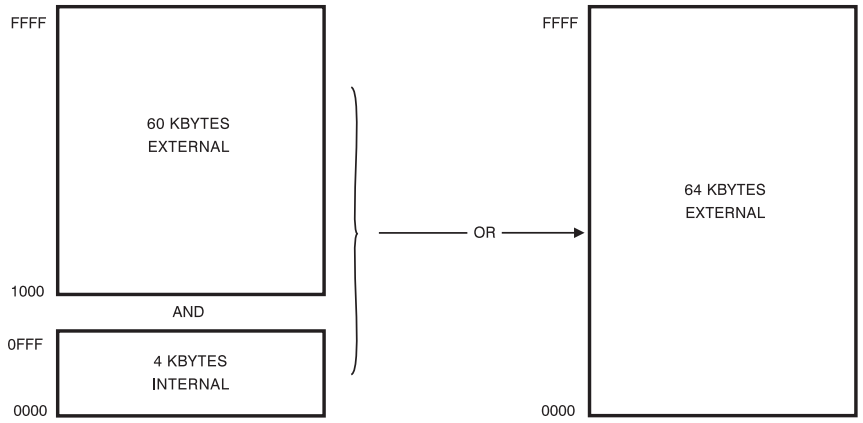
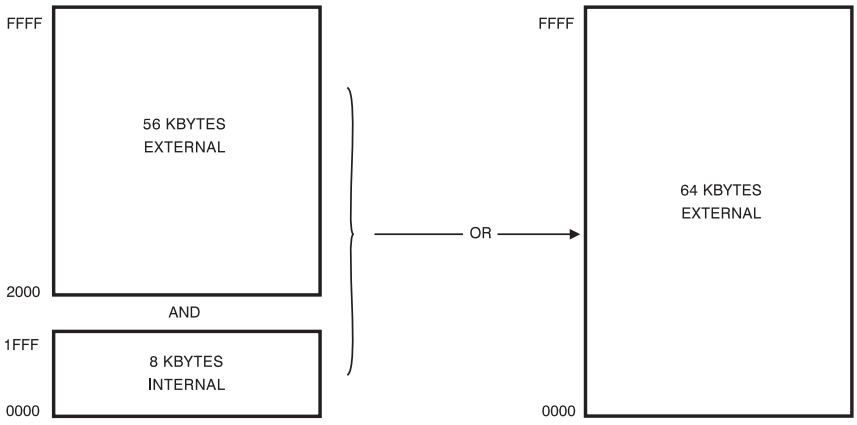


Figure 2. AT89C52 Program Memory



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Data Memory

The AT89C can directly address up to 64K bytes of data memory external to the chip. The MOVX instruction accesses the external data memory. (Refer to the Instruction Set section in this chapter for a detailed description of instructions).

The AT89C51 has 128 bytes of on-chip RAM (256 bytes in the AT89C52) plus a number of Special Function Registers (SFRs). The lower 128 bytes of RAM can be accessed either by direct addressing (MOV data addr) or by indirect addressing (MOV @Ri). Figure 3 shows the AT89C51 and the AT89C52 data memory organization.

Figure 3. A: The AT89C51 Data Memory

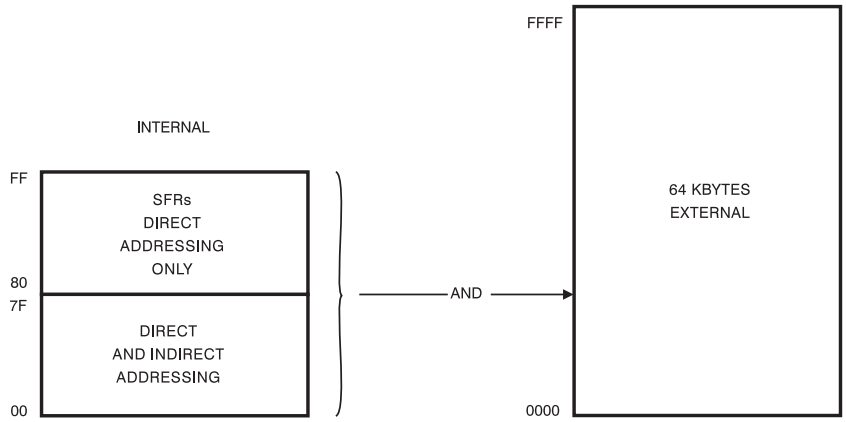
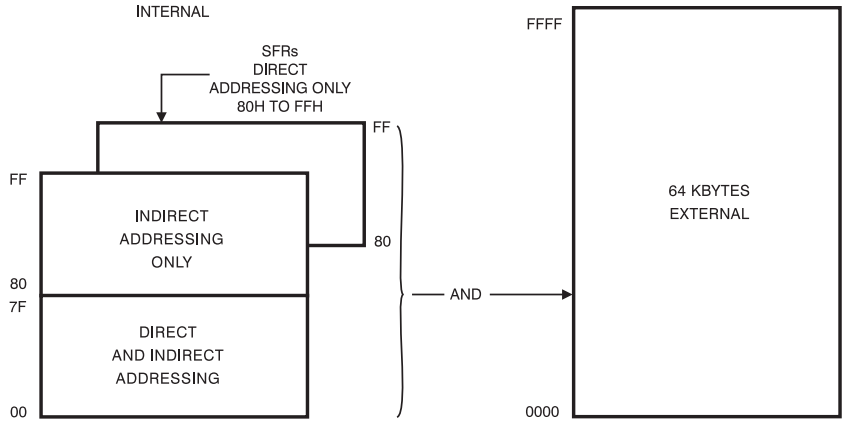


Figure 3. B: The AT89C52 Data Memory



Indirect Address Area

In Figure 3b, the SFRs and the indirect address RAM have the same addresses (80H through 0FFH). Nevertheless, they are two separate areas and are accessed in two different ways.

For example, the following instruction writes 0AAH to Port 0, which is one of the SFRs.

```
MOV 80H, # 0AAH
```

The following instruction writes 0BBH in location 80H of the data RAM.

```
MOVR0, # 80H
MOV@ R0, # 0BBH
```

Thus, after executing both of these instructions, Port 0 contains 0AAH, and location 80H of the RAM contains 0BBH.

The stack operations are examples of indirect addressing, so the upper 128 bytes of data RAM are available as stack space in devices that implement 256 bytes of internal RAM.

Direct and Indirect Address Area

The 128 bytes of RAM that can be accessed by both direct and indirect addressing can be divided into 3 segments as described in this section and as shown in Figure 4.

1. Register Banks 0-3: Locations 0 through 1FH (32 bytes). Reset default is to register bank 0. To use the other register banks, the user must select them in the software. Each register bank contains eight 1-byte registers, 0 through 7.

Reset initializes the Stack Pointer to location 07H. The Stack Pointer is then incremented once to start from location 08H, which is the first register (R0) of the second register bank. Thus, in order to use more than one register bank, the SP should be initialized to a different location of the RAM that is not used for data storage (that is, a higher part of the RAM).

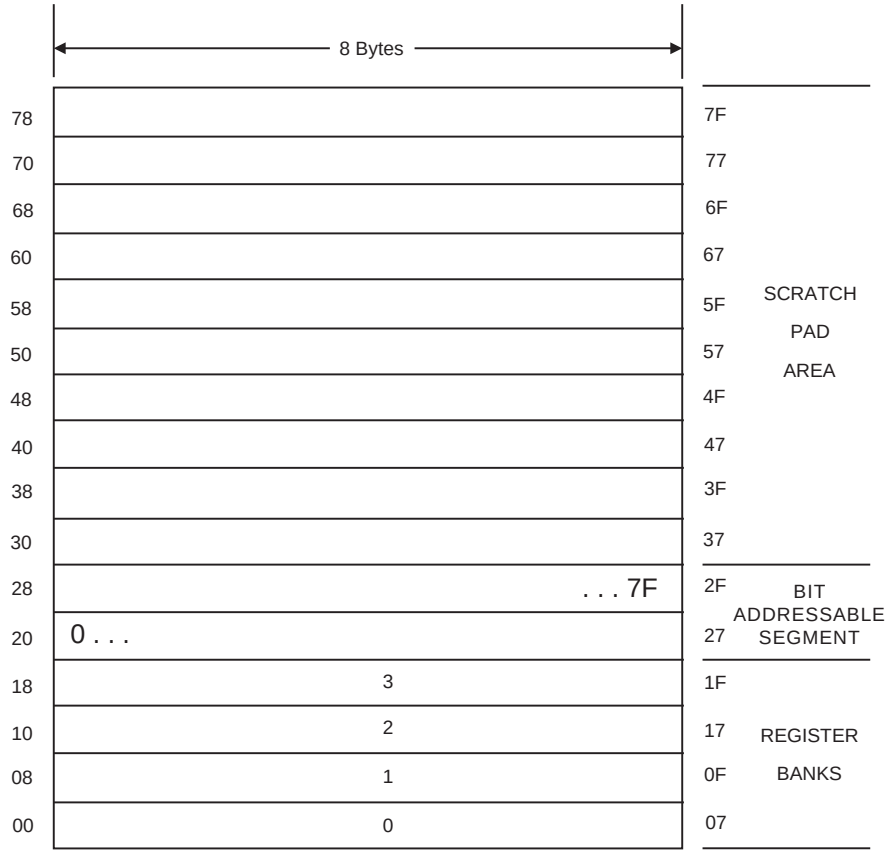
2. Bit Addressable Area: 16 bytes have been assigned for this segment, 20H through 2FH. Each of the 128 bits of this segment can be directly addressed (0 through 7FH).

These bits can be referred to in two ways. One way is to refer to their addresses, that is, 0 to 7FH. The other way is with reference to bytes 20H to 2FH. Thus, bits 0 through 7 can also be referred to as bits 20.0 through 20.7, and bits 8 through FH are the same as 21.0 through 21.7, and so on.

Each of the 16 bytes in this segment can also be addressed as a byte.

3. Scratch Pad Area: Bytes 30H through 7FH are available to the user as data RAM. However, if the stack pointer has been initialized to this area, enough bytes should be left aside to prevent SP data destruction.

Figure 4. 128 Bytes of Directly and Indirectly Addressable RAM



Special Function Registers

Table 1 contains a list of all the SFRs and their addresses.

All of the SFRs that are byte- and bit-addressable are located on the first column of the diagram in Figure 5.

Table 1. Special Function Registers

Symbol	Name	Address
ACC(1)	Accumulator	0E0H
B(1)	B Register	0F0H
PSW(1)	Program Status Word	0D0H
SP	Stack Pointer	81H
DPTR	Data Pointer 2 Bytes	
DPL	Low Byte	82H
DPH	High Byte	83H
P0(1)	Port 0	80H
P1(1)	Port 1	90H
P2(1)	Port 2	0A0H
P3(1)	Port 3	0B0H
IP(1)	Interrupt Priority Control	0B8H
IE(1)	Interrupt Enable Control	0A8H
TMOD	Timer/Counter Mode Control	89H
TCON(1)	Timer/Counter Control	88H
T2CON(1)(2)	Timer/Counter 2 Control	0C8H
T2MOD(2)	Timer/Counter 2 Mode Control	0C9H
TH0	Timer/Counter 0 High Byte	8CH
TL0	Timer/Counter 0 Low Byte	8AH
TH1	Timer/Counter 1 High Byte	8DH
TL1	Timer/Counter 1 Low Byte	8BH
TH2(2)	Timer/Counter 2 High Byte	0CDH
TL2(2)	Timer/Counter 2 Low Byte	0CCH
RCAP2H(2)	T/C 2 Capture Reg. High Byte	0CBH
RCAP2L(2)	T/C 2 Capture Reg. Low Byte	0CAH
SCON(1)	Serial Control	98H
SBUF	Serial Data Buffer	99H
PCON	Power Control	87H

Notes: 1. Bit addressable
2. AT89C52 only

Contents of the SFRs Just After Power-On or a Reset

Table 2. Contents of the SFRs after power-on or a hardware reset

Register	Value in Binary
ACC(2)	00000000
B(2)	00000000
PSW(2)	00000000
SP	00000111
DPTR	
DPH	00000000
DPL	00000000
PO(2)	11111111
P1(2)	11111111
P2(2)	11111111
P3(2)	11111111
IP(2)	80C51 XXX00000, 80C52 XX000000
IE(2)	80C51 0XX00000, 80C52 0X000000
TMOD	00000000
T2MOD(3)	XXXXXX00
TCON(2)	00000000
T2CON(2)(3)	00000000
TH0	00000000
TL0	00000000
TH1	00000000
TL1	00000000
TH2(3)	00000000
TL2(3)	00000000
RCAP2H(3)	00000000
RRAP2L(3)	00000000
SCON(2)	00000000
SBUF	Indeterminate
PCON	CMOS 0XXX0000

Notes: 1. X = Undefined
2. Bit Addressable
3. AT89C52 only

Special Function Register Map

Figure 5. SFR Memory Map

	8 Bytes								
F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW(1)								D7
C8	T2CON(1)(2)	T2MOD(2)	RCAP2L(2)	RCAP2H(2)	TL2(2)	TH2(2)			CF
C0									C7
B8	IP(1)								BF
B0	P3								B7
A8	IE(1)								AF
A0	P2								A7
98	SCON(1)	SBUF							9F
90	P1								97
88	TCON(1)	TMOD(1)	TL0	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON(1)	87

↑ Bit Addressable

Notes: 1. SFRs converting mode or control bits
2. AT89C52 only

SFRs whose bits are assigned for various functions are listed in this section. For more detailed information, refer to the Microcontroller Architectural Overview chapter of this book.

PSW: Program Status Word (Bit Addressable)

CY	AC	F0	RS1	RS0	OV	—	P

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.(1)
RS0	PSW.3	Register Bank selector bit 0. (1)
OV	PSW.2	Overflow flag.
—	PSW.1	User definable flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of 1 bits in the accumulator.

Note: 1. The values of RS0 and RS1 select the corresponding register bank.

RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

PCON: Power Control Register (Not Bit Addressable)

SMOD	—	—	—	GF1	GF0	PD	IDL

SMOD	Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD = 1, the baud rate is doubled when the Serial Port is used in modes 1, 2, or 3.
—	Not implemented, reserved for future use.(1)
—	Not implemented, reserved for future use.(1)
—	Not implemented, reserved for future use. (1)
GF1	General purpose flag bit.
GF0	General purpose flag bit.
PD	Power Down bit. Setting this bit activates Power Down operation in the AT89C51.
IDL	Idle Mode bit. Setting this bit activates Idle Mode operation in the AT89C51.

If 1s are written to PD and IDL at the same time, PD takes precedence.

Note: 1. User software should not write 1s to reserved bits. These bits may be used in future microcontrollers to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

Interrupts

In order to use any of the interrupts in the Flash microcontroller, take the following three steps.

1. Set the EA (enable all) bit in the IE register to 1.
2. Set the corresponding individual interrupt enable bit in the IE register to 1.
3. Begin the interrupt service routine at the corresponding Vector Address of that interrupt. See the following table.

Interrupt Source	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
R1 & T1	0023H
TF2 & EXF2(1)	002BH

Note: 1. AT89C52 only.

In addition, for external interrupts, pins $\overline{INT0}$ and $\overline{INT1}$ (P3.2 and P3.3) must be set to 1, and depending on whether the interrupt is to be level or transition activated, bits IT0 or IT1 in the TCON register may need to be set to 1.

ITx = 0 level activated

ITx = 1 transition activated

IE: Interrupt Enable Register (Bit Addressable)

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	—	ET2	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
—	IE.6	Not implemented, reserved for future use.(1)
ET2	IE.5	Enables or disables the Timer 2 overflow or capture interrupt (AT89C52 only).
ES	IE.4	Enables or disables the serial port interrupt.
ET1	IE.3	Enables or disables the Timer 1 overflow interrupt.
EX1	IE.2	Enables or disables External Interrupt 1.
ET0	IE. 1	Enables or disables the Timer 0 overflow interrupt.
EX0	IE.0	Enables or disables External Interrupt 0.

Note: 1. User software should not write 1s to reserved bits. These bits may be used in future Flash microcontrollers to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

Assigning Higher Priority to One or More Interrupts

In order to assign higher priority to an interrupt the corresponding bit in the IP register must be set to 1.

While an interrupt service is in progress, it cannot be interrupted by an interrupt of the same or lower priority.

Priority Within Level

The only purpose of priority within a level is to resolve simultaneous requests of the same priority level.

From high to low, interrupt sources are listed below.

IE0

TF0

IE1

TF1

RI or TI

TF2 or EXF2

IP: Interrupt Priority Register (Bit Addressable)

If the bit is 0, the corresponding interrupt has a lower priority. If the bit is 1, the corresponding interrupt has a higher priority

—	—	PT2	PS	PT1	PX1	PT0	PX0

—	IP. 7	Not implemented, reserved for future use.(1)
—	IP. 6	Not implemented, reserved for future use.(1)
PT2	IP. 5	Defines the Timer 2 interrupt priority level (AT89C52 only).
PS	IP. 4	Defines the Serial Port interrupt priority level.
PT1	IP. 3	Defines the Timer 1 interrupt priority level.
PX1	IP. 2	Defines External Interrupt 1 priority level.
PT0	IP. 1	Defines the Timer 0 interrupt priority level.
PX0	IP. 0	Defines the External Interrupt 0 priority level.

Note: 1. User software should not write 1s to reserved bits. These bits may be used in future Flash microcontrollers to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

TCON: Timer/Counter Control Register (Bit Addressable)

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1	TCON. 7	Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as the processor vectors to the interrupt service routine.
TR1	TCON. 6	Timer 1 run control bit. Set/cleared by software to turn Timer/Counter 1 ON/OFF.
TF0	TCON. 5	Timer 0 overflow flag. Set by hardware when the Timer/Counter 0 overflows. Cleared by hardware as the processor vectors to the service routine.
TR0	TCON. 4	Timer 0 run control bit. Set/cleared by software to turn Timer/Counter 0 ON/OFF.
IE1	TCON. 3	External Interrupt 1 edge flag. Set by hardware when the External Interrupt edge is detected. Cleared by hardware when the interrupt is processed.
IT1	TCON. 2	Interrupt 1 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.
IE0	TCON. 1	External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed.
IT0	TCON. 0	Interrupt 0 type control bit. Set/cleared by software to specify falling edge/low level triggered External Interrupt.

TMOD: Timer/Counter Mode Control Register (Not Bit Addressable)

Timer 1				Timer 0			
GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

GATE	When TRx (in TCON) is set and GATE = 1, TIMER/COUNTERx runs only while the INTx pin is high (hardware control). When GATE = 0, TIMER/COUNTERx will run only while TRx = 1 (software control).
C/$\overline{T}$	Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from Tx input pin).
M1	Mode selector bit.(1)
M0	Mode selector bit.(1)

Note: 1.

M1	M0	Operating Mode	
0	0	0	13-bit Timer
0	1	1	16-bit Timer/Counter
1	0	2	8-bit Auto-Reload Timer/Counter
1	1	3	Split Timer Mode: (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, TH0 is an 8-bit Timer and is controlled by Timer 1 control bits.
1	1	3	(Timer 1) Timer/Counter 1 stopped.

Timer Set-Up

Tables 3 through 6 give TMOD values that can be used to set up Timer 0 in different modes.

It is assumed that only one timer is used at a time. If Timers 0 and 1 must run simultaneously in any mode, the value in TMOD for Timer 0 must be ORed with the value shown for Timer 1 (Tables 5 and 6).

For example, if Timer 0 must run in mode 1 GATE (external control), and Timer 1 must run in mode 2 COUNTER, then the value that must be loaded into TMOD is 69H (09H from Table 3 ORed with 60H from Table 6).

Moreover, it is assumed that the user is not ready at this point to turn the timers on and will do so at another point in the program by setting bit TRx (in TCON) to 1.

Timer/Counter 0

Table 3. Timer/Counter 0 Used as a Timer

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
0	13-bit Timer	00H	08H
1	16-bit Timer	01H	09H
2	8-bit Auto-Reload	02H	0AH
3	two 8-bit Timers	03H	0BH

Table 4. Timer/Counter 0 Used as a Counter

MODE	TIMER 0 FUNCTION	TMOD	
		INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
0	13-bit Timer	04H	0CH
1	16-bit Timer	05H	0DH
2	8-bit Auto-Reload	06H	0EH
3	one 8-bit Counter	07H	0FH

Notes: 1. The Timer is turned ON/OFF by setting/clearing bit TR0 in the software.

2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{INT0}$ (P3.2) when TR0 = 1 (hardware control).

Timer/Counter 1

Table 5. Timer/Counter 1 Used as a Timer

MODE	TIMER 1 FUNCTION	TMOD	
		INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
0	13-bit Timer	00H	80H
1	16-bit Timer	10H	90H
2	8-bit Auto-Reload	20H	A0H
3	does not run	30H	B0H

Table 6. Timer/Counter 1 Used as a Counter

MODE	COUNTER 1 FUNCTION	TMOD	
		INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
0	13-bit Timer	40H	C0H
1	16-bit Timer	50H	D0H
2	8-bit Auto-Reload	60H	E0H
3	not available	—	—

Notes: 1. The Timer is turned ON/OFF by setting/clearing bit TR1 in the software.

2. The Timer is turned ON/OFF by the 1 to 0 transition on $\overline{INT1}$ (P3.3) wen TR1 = 1 (hardware control).

T2CON: Timer/Counter 2 Control Register (Bit Addressable)

AT89C52 Only

TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$

TF2	T2CON. 7	Timer 2 overflow flag set by hardware and cleared by software. TF2 cannot be set when either RCLK = 1 or CLK = 1
EXF2	T2CON. 6	Timer 2 external flag set when either a capture or reload is caused by a negative transition on T2EX, and EXEN2 = 1. When Timer 2 interrupt is enabled, EXF2 = 1 causes the CPU to vector to the Timer 2 interrupt routine. EXF2 must be cleared by software.
RCLK	T2CON. 5	Receive clock flag. When set, causes the Serial Port to use Timer 2 overflow pulses for its receive clock in modes 1 and 3. RCLK = 0 causes Timer 1 overflow to be used for the receive clock.
TLCK	T2CON. 4	Transmit clock flag. When set, causes the Serial Port to use Timer 2 overflow pulses for its transmit clock in modes 1 and 3. TCLK = 0 causes Timer 1 overflows to be used for the transmit clock.
EXEN2	T2CON. 3	Timer 2 external enable flag. When set, allows a capture or reload to occur as a result of negative transition on T2EX if Timer 2 is not being used to clock the Serial Port. EXEN2 = 0 causes Timer 2 to ignore events at T2EX.
TR2	T2CON. 2	Software START/STOP control for Timer 2. A logic 1 starts the Timer.
C/$\overline{T2}$	T2CON. 1	Timer or Counter select. 0 = Internal Timer. 1 = External Event Counter (triggered by falling edge).
CP/$\overline{RL2}$	T2CON. 0	Capture/Reload flag. When set, captures occur on negative transitions at T2EX if EXEN2 = 1. When cleared, auto-reloads occur either with Timer 2 overflows or negative transitions at T2EX when EXEN2 = 1. When either RCLK = 1 or TCLK = 1, this bit is ignored and the Timer is forced to auto-reload on Timer 2 overflow.

T2MOD: Timer 2 Mode Control Register

T2MOD Address = 0C9H **Reset Value = XXXX XX00B**

Not Bit Addressable

-	-	-	-	-	-	T2OE	DCEN
Bit 7	6	5	4	3	2	1	0

Symbol	Function
-	Not implemented, reserved for future use
T2OE	Timer 2 Output Enable bit
DCEN	When set, this bit allows Timer 2 to be configured as an up/down counter.

Timer/Counter 2 Set-Up

Except for the baud rate generator mode, the values given for T2CON do not include the setting of the TR2 bit. Therefore, bit TR2 must be set separately to turn the Timer on.

Table 7. Timer/Counter 2 Used as a Timer

MODE	T2CON	
	INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
16-bit Auto-Reload	00H	08H
16-bit Capture	01H	09H
Baud rate generator receive and transmit same baud rate	34H	36H
receive only	24H	26H
transmit only	14H	16H

Table 8. Timer/Counter 2 Used as a Counter

MODE	TMOD	
	INTERNAL CONTROL(1)	EXTERNAL CONTROL(2)
16-bit Auto Reload	02H	0AH
16-bit Capture	03H	0BH

Notes:
1. Capture/Reload occurs only on Timer/Counter overflow.
2. Capture/Reload occurs on Timer/Counter overflow and a 1 to 0 transition on T2EX (P1.1) pin except when Timer 2 is used in the baud rate generating mode.

SCON: Serial Port Control Register (Bit Addressable)

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

SM0	SCON. 7	Serial Port mode specifier. (1)
SM1	SCON. 6	Serial Port mode specifier. (1)
SM2	SCON. 5	Enables the multiprocessor communication feature in modes 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI is not activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI is not activated if a valid stop bit was not received. In mode 0, SM2 should be 0. (See Table 9).
REN	SCON. 4	Set/Cleared by software to Enable/Disable reception.
TB8	SCON. 3	The 9th bit that is transmitted in modes 2 and 3. Set/Cleared by software.
RB8	SCON. 2	In modes 2 and 3, is the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	SCON. 1	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes. Must be cleared by software.
RI	SCON. 0	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0 or halfway through the stop bit time in the other modes (except see SM2). Must be cleared by software.

Note: 1.

SM0	SM1	Mode	Description	Baud Rate
0	0	0	SHIFT REGISTER	Fosc./12
0	1	1	8-Bit UART	Variable
1	0	2	9-Bit UART	Fosc./64 OR Fosc./32
1	1	3	9-Bit UART	Variable

Table 9. Serial Port Set-Up

MODE	SCON	SM2 VARIATION
0 1 2 3	10H 50H 90H D0H	Single Processor Environment (SM2 = 0)
0 1 2 3	NA 70H B0H F0H	Multiprocessor Environment (SM2 = 1)

Generating Baud Rates

Serial Port in Mode 0

Mode 0 has a fixed baud rate, which is 1/12 of the oscillator frequency. To run the serial port in this mode, none of the Timer/Counters need to be set up. Only the SCON register needs to be defined.

$$\text{Baud Rate} = \frac{\text{Oscillator Frequency}}{12}$$

Serial Port in Mode 1

Mode 1 has a variable baud rate. The baud rate can be generated by either Timer 1 or Timer 2 (AT89C52 only).

Using Timer/Counter 1 to Generate Baud Rates

For this purpose, Timer l is used in mode 2 (Auto-Reload). Refer to the Timer Setup section of this chapter.

$$\text{Baud Rate} = \frac{K \times \text{Oscillator Frequency}}{32 \times 12 \times [256 - (TH1)]}$$

If SMOD = 0, then K = 1.

If SMOD = 1, then K = 2. (SMOD is the PCON register).

The user usually knows the baud rate but needs to know the reload value for TH1. Therefore, the equation to calculate TH1 can be written as follows.

$$TH1 = 256 - \frac{K \times \text{Oscillator Frequency}}{384 \times \text{Baud Rate}}$$

TH1 must be an integer value. Rounding off TH1 to the nearest integer may not produce the desired baud rate. In this case, the user may have to choose another crystal frequency. See Baud Rate table.

Since the PCON register is not bit addressable, one way to set the bit is logical ORing the PCON register (that is, ORL PCON, # 80H). The address of PCON is 87H.

Using Timer/Counter 2 to Generate Baud Rates

For this purpose, Timer 2 must be used in the baud rate generating mode. Refer to Timer 2 Setup Table in this chapter. If Timer 2 is clocked through pin T2 (P1.0) the baud rate given by the following equation.

$$\text{Baud Rate} = \frac{\text{Timer 2 Overflow Rate}}{16}$$

If it is being clocked internally the baud rate is given by the following equation.

$$\text{Baud Rate} = \frac{\text{Oscillator Frequency}}{32 \times [65536 - (RCAP2H,RCAP2L)]}$$

To obtain the reload value for RCAP2H and RCAP2L the previous equation can be rewritten as follows.

$$RCAP2H,RCAP2L = 65536 - \frac{\text{Oscillator Frequency}}{32 \times \text{Baud Rate}}$$

Serial Port in Mode 2

The baud rate is fixed in this mode and is 1/32 or 1/64 of the oscillator frequency, depending on the value of the SMOD bit in the PCON register.

In this mode, none of the Timers is used, and the clock comes from the internal phase 2 clock.

SMOD = 1, Baud Rate = 1/32 Osc Freq.

SMOD = O, Baud Rate = 1/64 Osc Freq.

To set the SMOD bit, use ORL PCON, # 80H. The address of PCON is 87H.

Serial Port in Mode 3

The baud rate in mode 3 is variable and sets up exactly the same as in mode 1.

Baud Rate Table

Crystal Frequency	7.3728 MHz	8.00 MHz	11.0592 MHz	12.00 MHz	14.75156 MHz	16.00 MHz
TH1						
E0	600	651	900	976	1,200	1,302
F0	1,200	1,302	1,800	1,953	2,400	2,604
F8	2,400	2,604	3,600	3,906	4,800	5,208
F9	2,743	2,976	8,299	4,464	5,486	5,952
FA	3,200	3,472	9,600	5,208	6,400	6,944
FF	19,200	20,833	57,600	62,500		41,666

Table 10. Baud Rate Summary

Baud Rate	Crystal Frequency	SMOD	TH1 Reload Value	Actual Baud Rate	Error
9600	12.000 MHz	1	-7 (F9H)	8923	7%
2400	12.000 MHz	0	-13 (F3H)	2404	0.16%
1200	12.000 MHz	0	-26 (E6H)	1202	0.16%
9200	11.059 MHz	1	-3 (FDH)	19200	0
9600	11.059 MHz	0	-3 (FDH)	9600	0
2400	11.059 MHz	0	-12 (F4H)	2400	0
1200	11.059 MHz	0	-24 (E8H)	1200	0

Note: Due to rounding, there is a slight error in the resulting baud rate. Generally, a 5% error is tolerable using asynchronous (start/stop) communications. Exact baud rates are possible using an 11.059 MHz crystal. The table above summarizes the TH1 reload values for the most common baud rates, using a 12.000 MHz or 11.059 MHz crystal.