

Fig. 6-1 Conventional and Array Logic Symbols for OR Gate

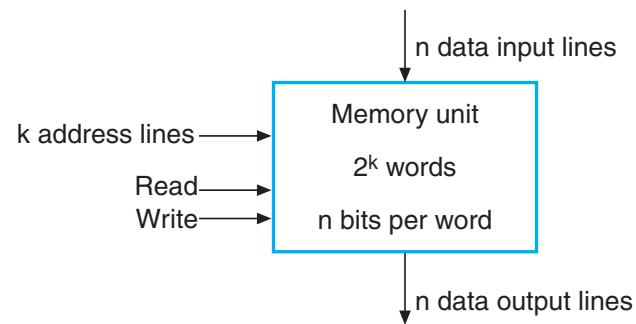


Fig. 6-2 Block Diagram of Memory

Memory address		Memory contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	.	.
	.	.
	.	.
	.	.
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

Fig. 6-3 Contents of a  $1024 \times 16$  Memory

**TABLE 6-1**  
**Control Inputs to a Memory Chip**

Chip select CS	Read/Write R/ $\overline{W}$	Memory operation
0	×	None
1	0	Write to selected word
1	1	Read from selected word

Table 6-1 Control Inputs to a Memory Chip

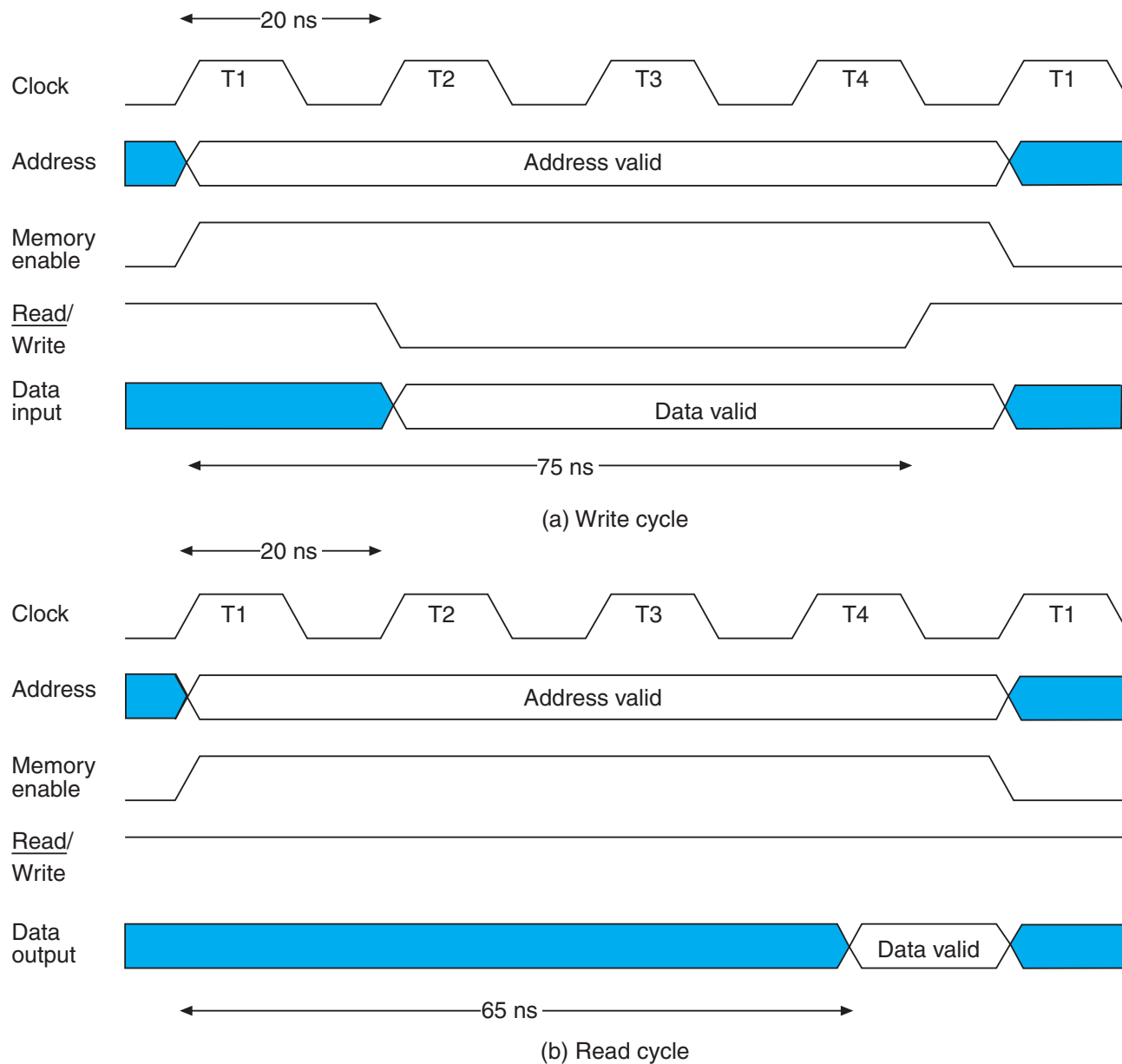


Fig. 6-4 Memory Cycle Timing Waveforms

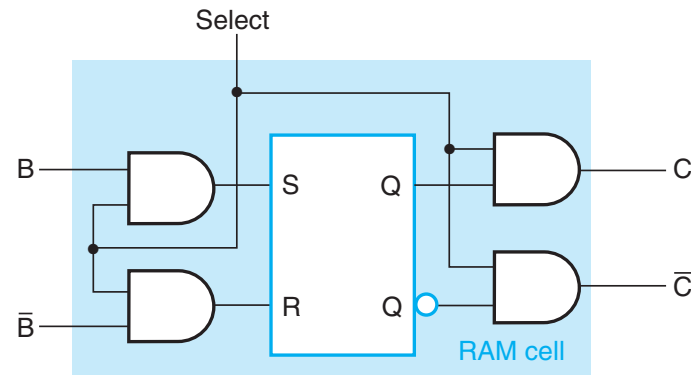
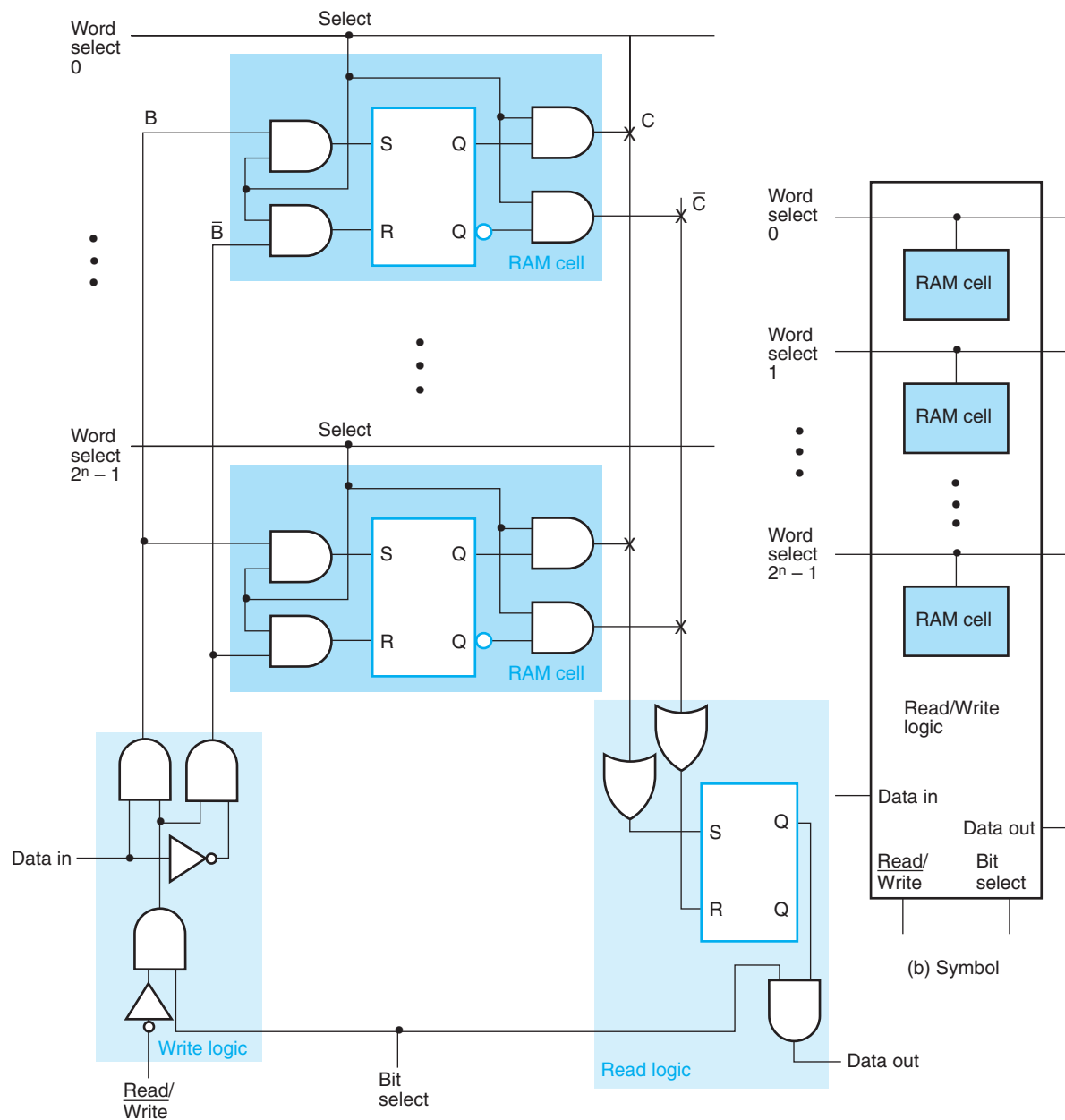


Fig. 6-5 Static RAM Cell



(a) Logic diagram

Fig. 6-6 RAM Bit Slice Model

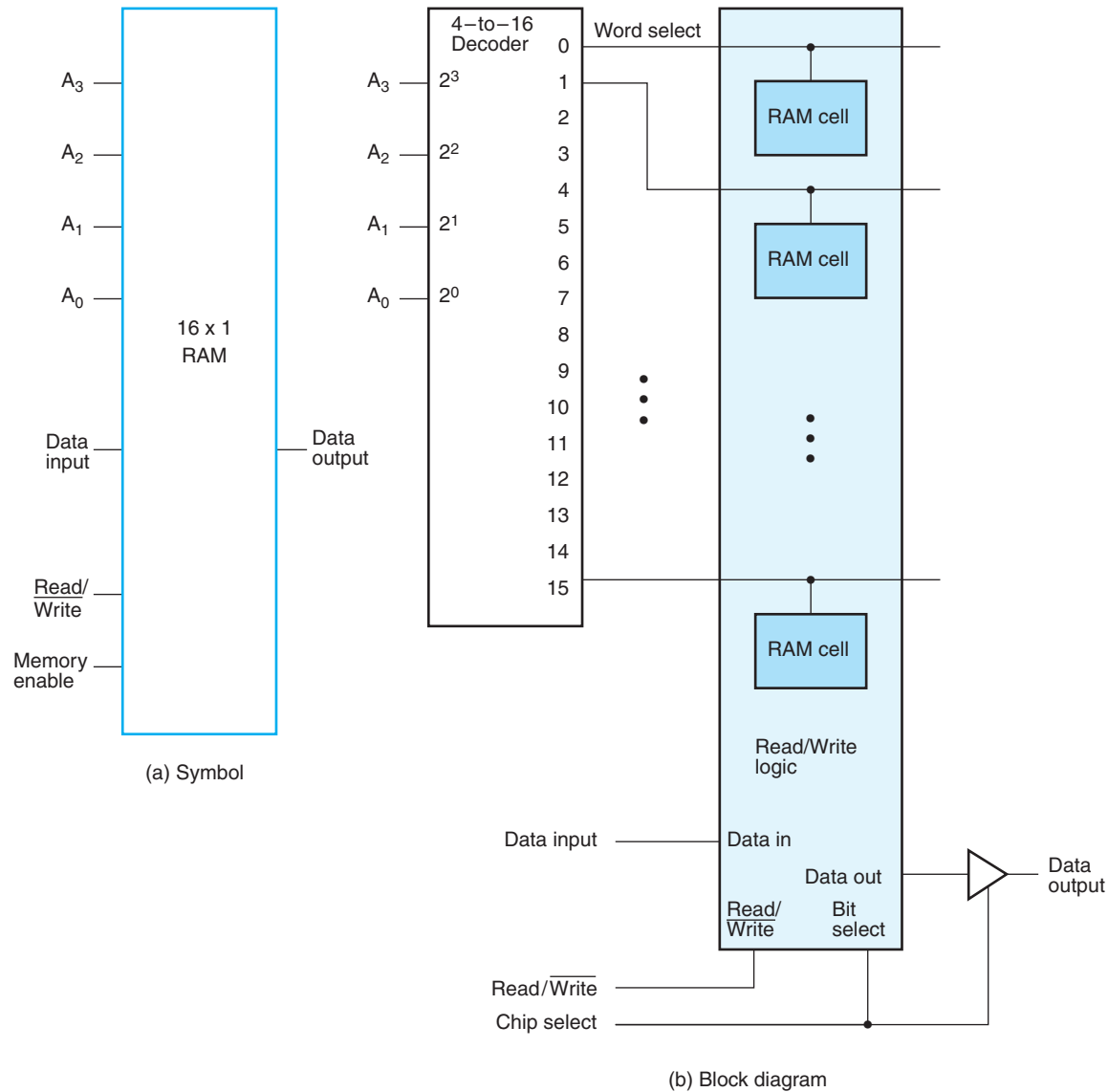
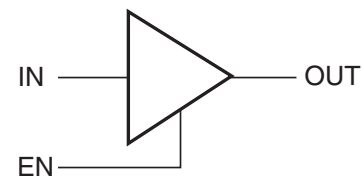


Fig. 6-7 16-Word by 1-Bit RAM Chip





(a) Logic symbol

EN	IN	OUT
0	X	Hi-Z
1	0	0
1	1	1

(b) Truth table

Fig. 6-8 Three-state Buffer

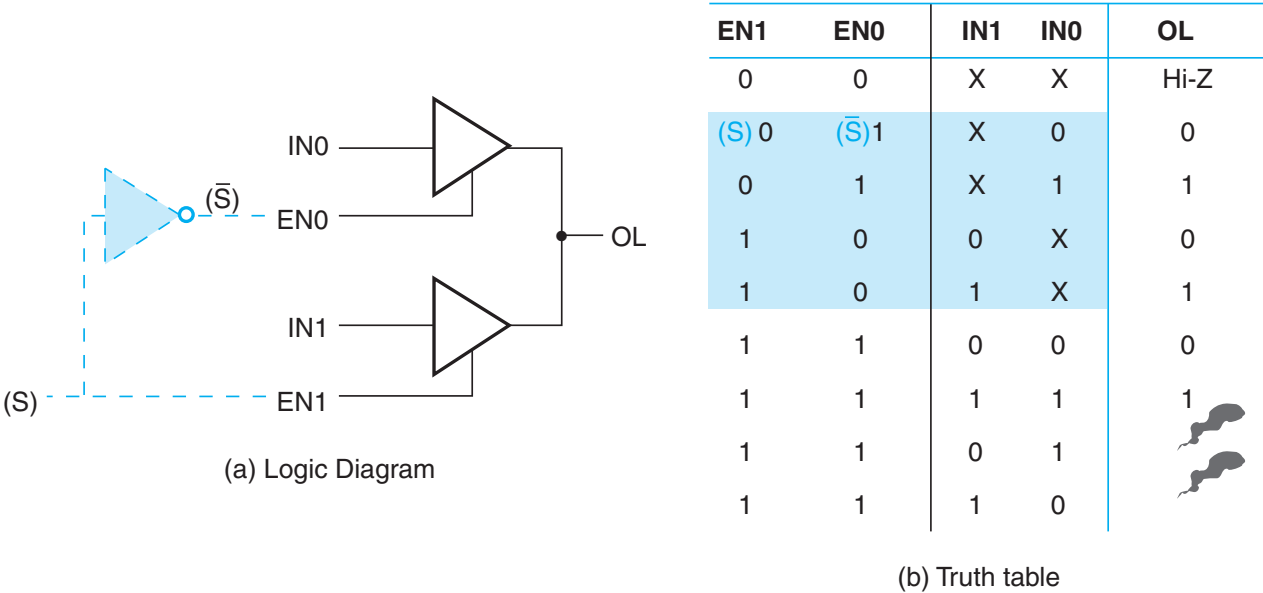


Fig. 6-9 Three-state Buffers Forming a Multiplexed Line OL

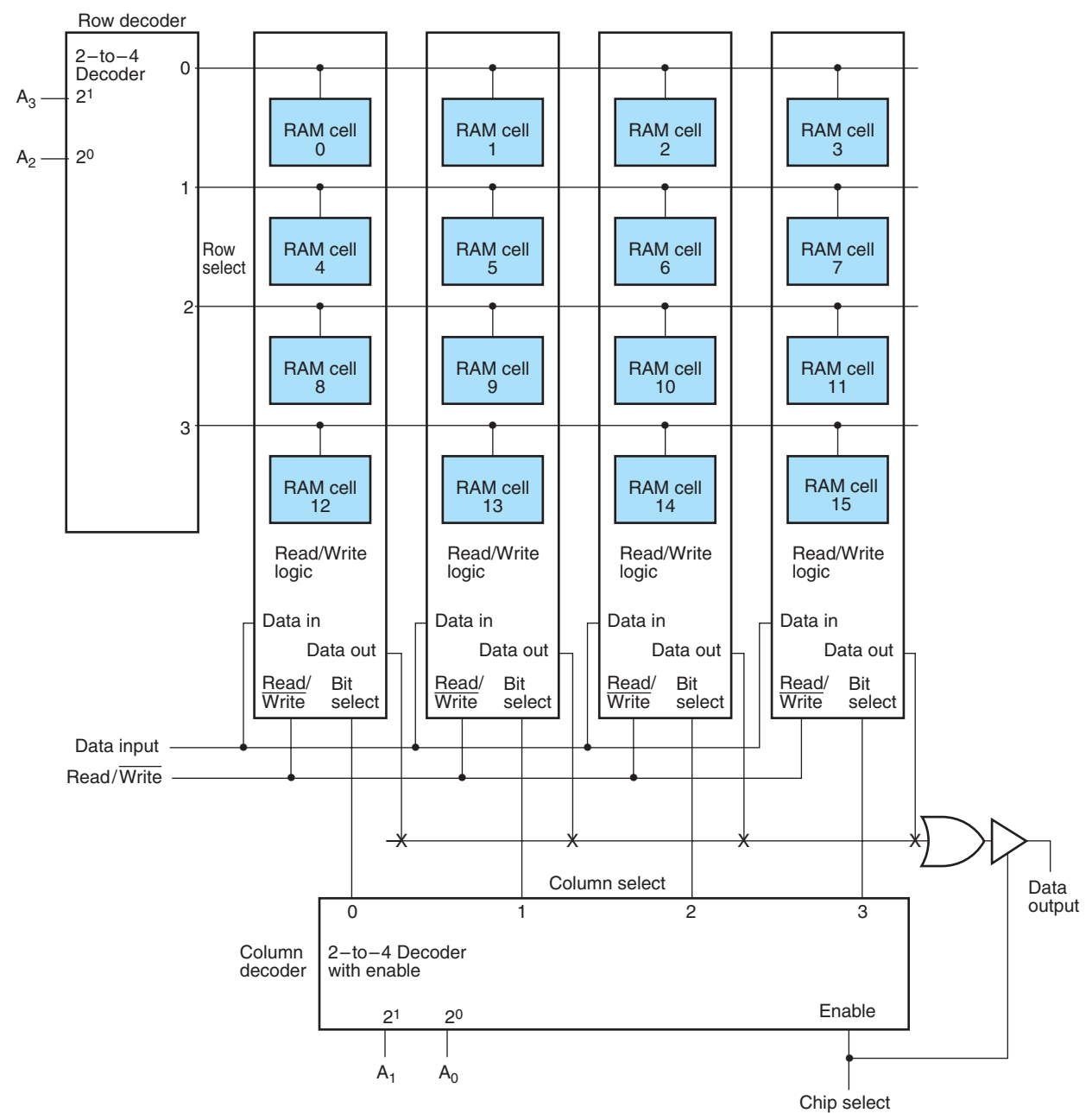
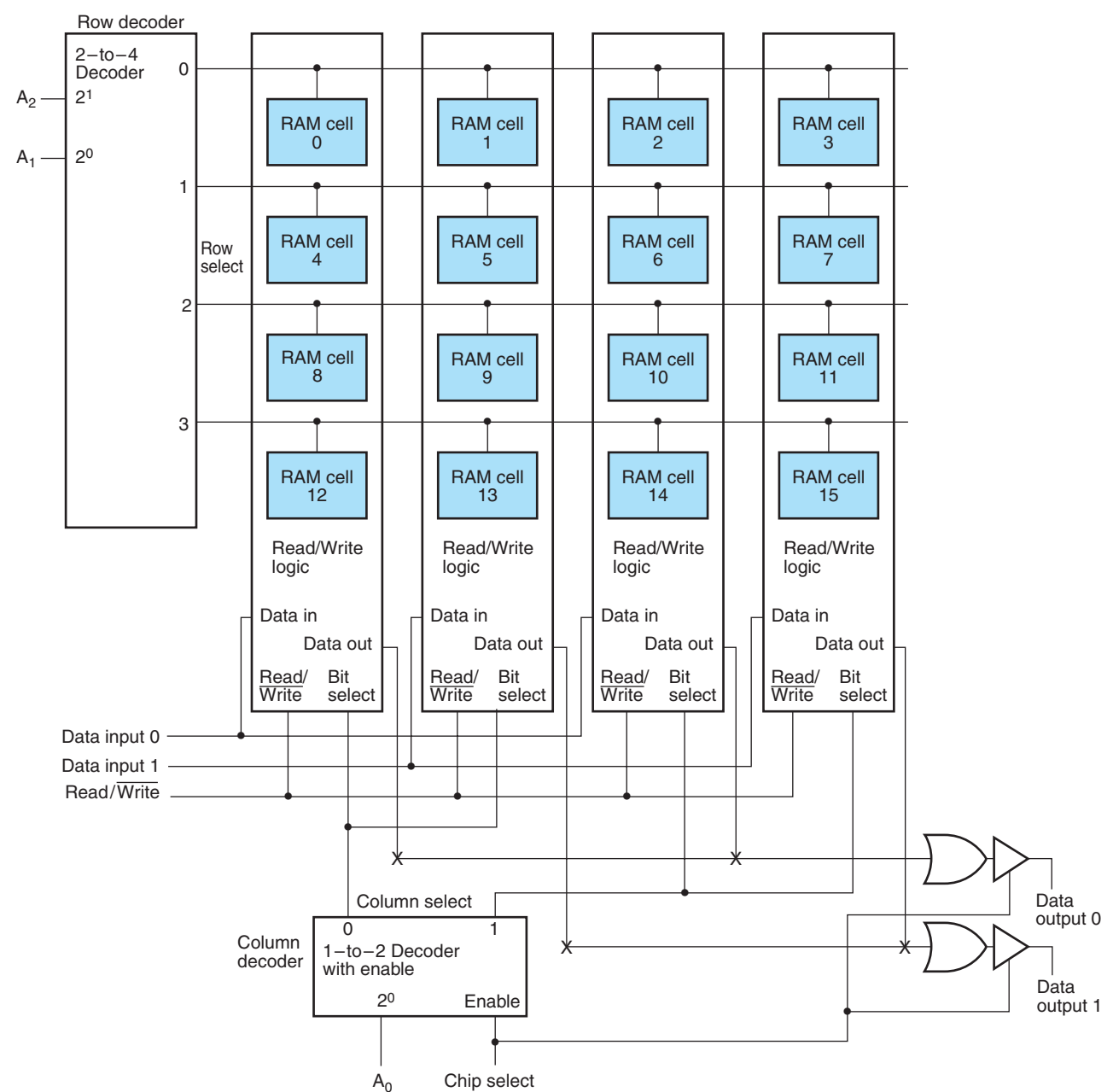


Fig. 6-10 Diagram of a 16 x 11 RAM Using a 4 x 4 RAM Cell Array



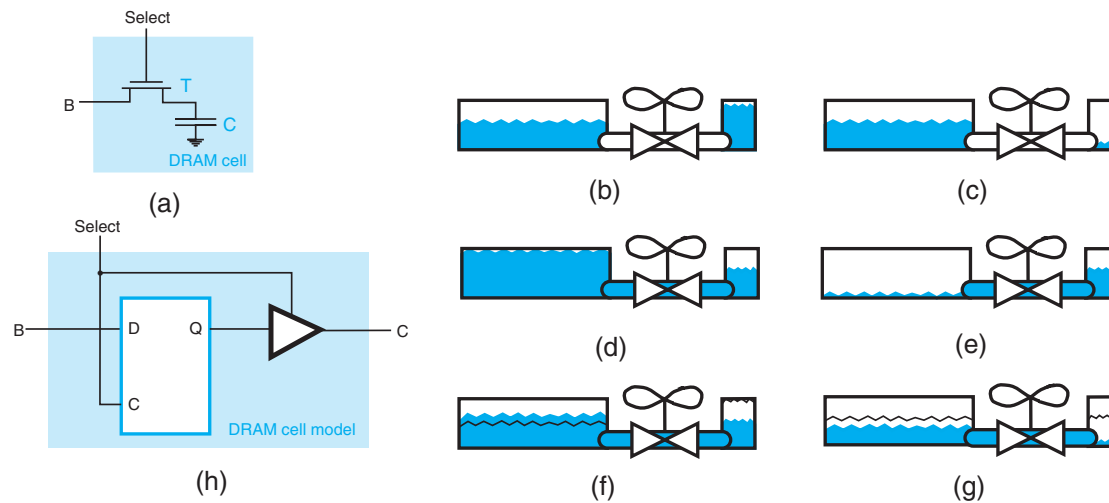


Fig. 6-12 Dynamic RAM Cell, Hydraulic Analogy of Cell Operation, and Cell Model

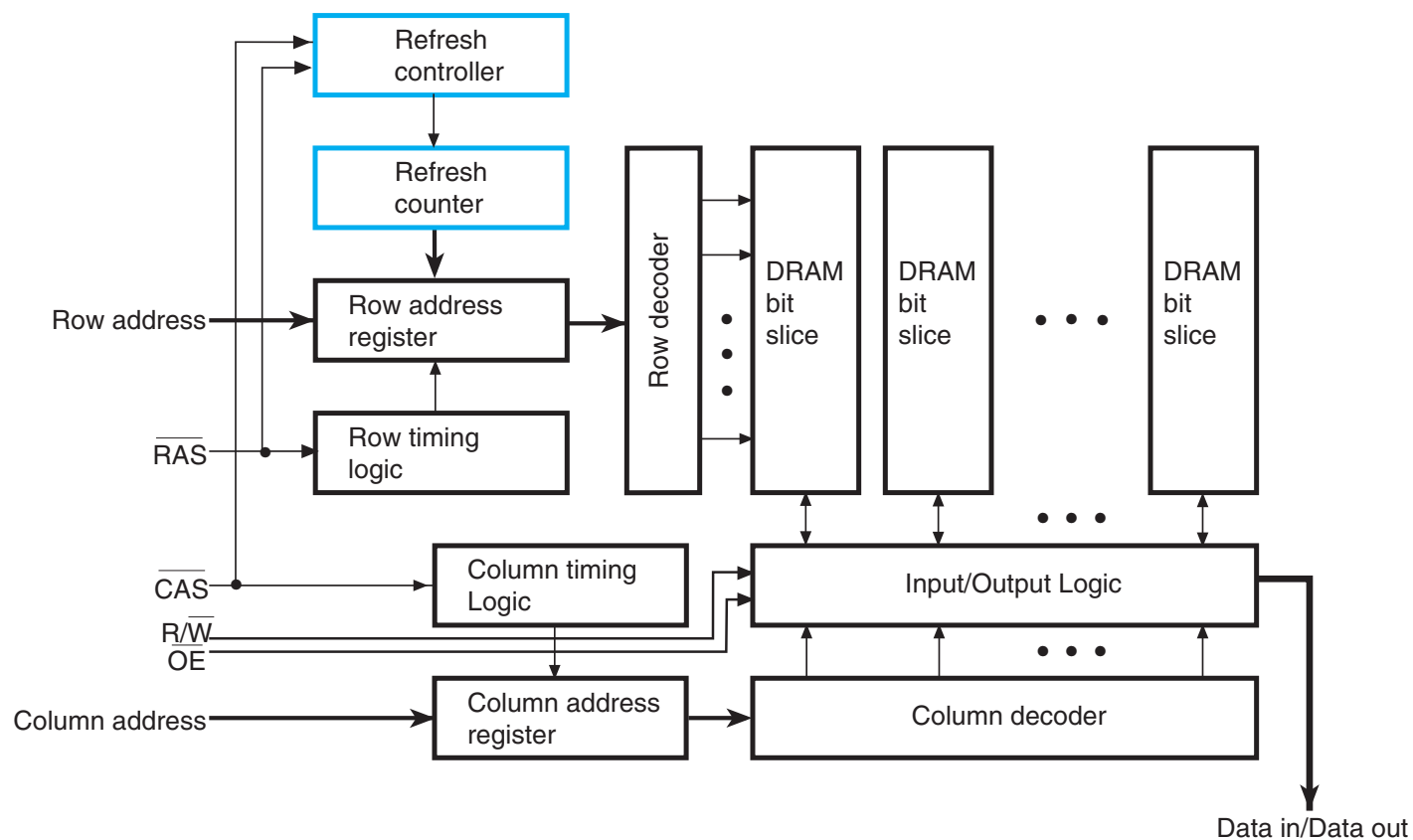
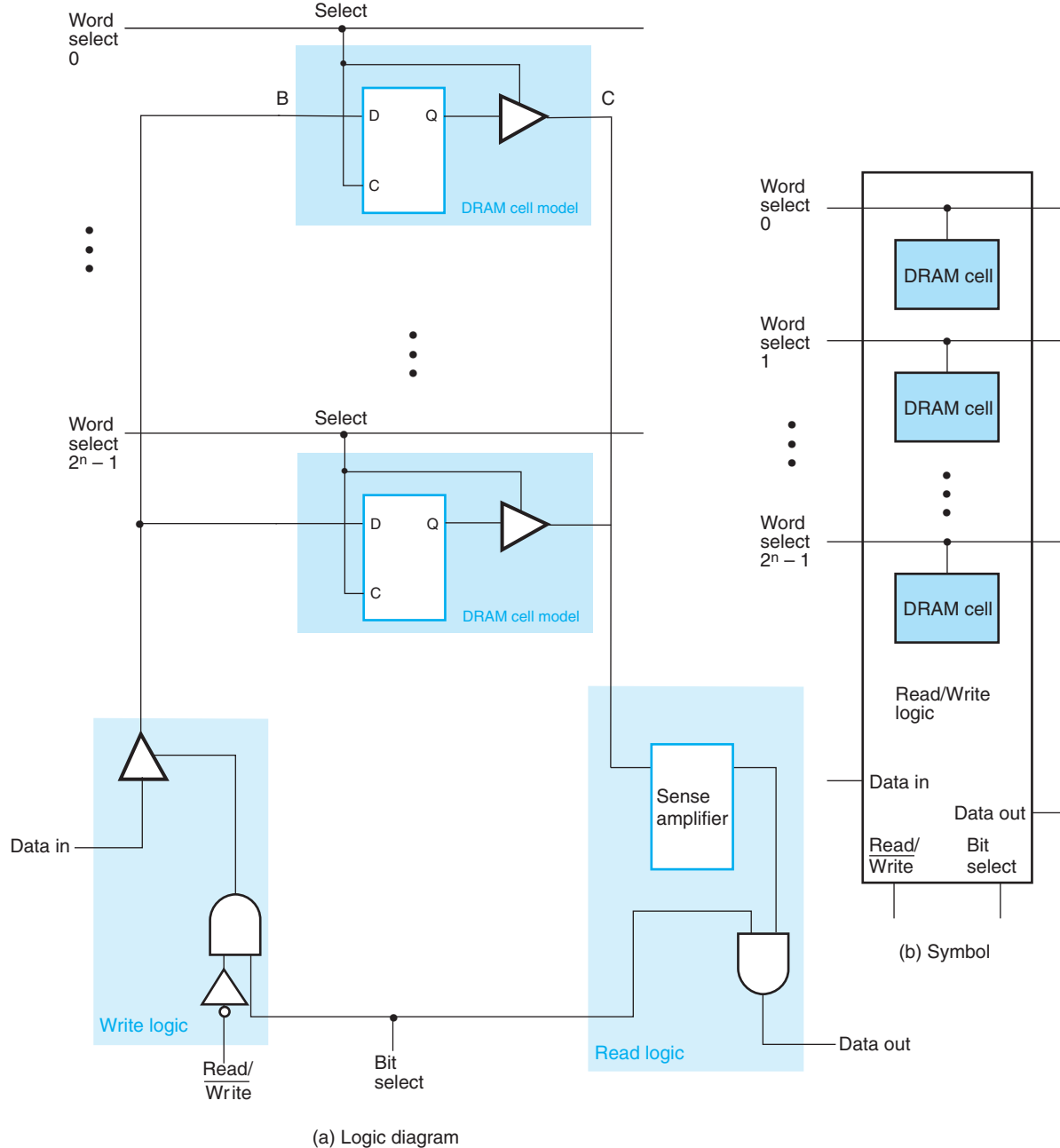


Fig. 6-13 Block Diagram of a DRAM Including Refresh Logic



(a) Logic diagram

(b) Symbol

Fig. 6-14 DRAM Bit Slice Model

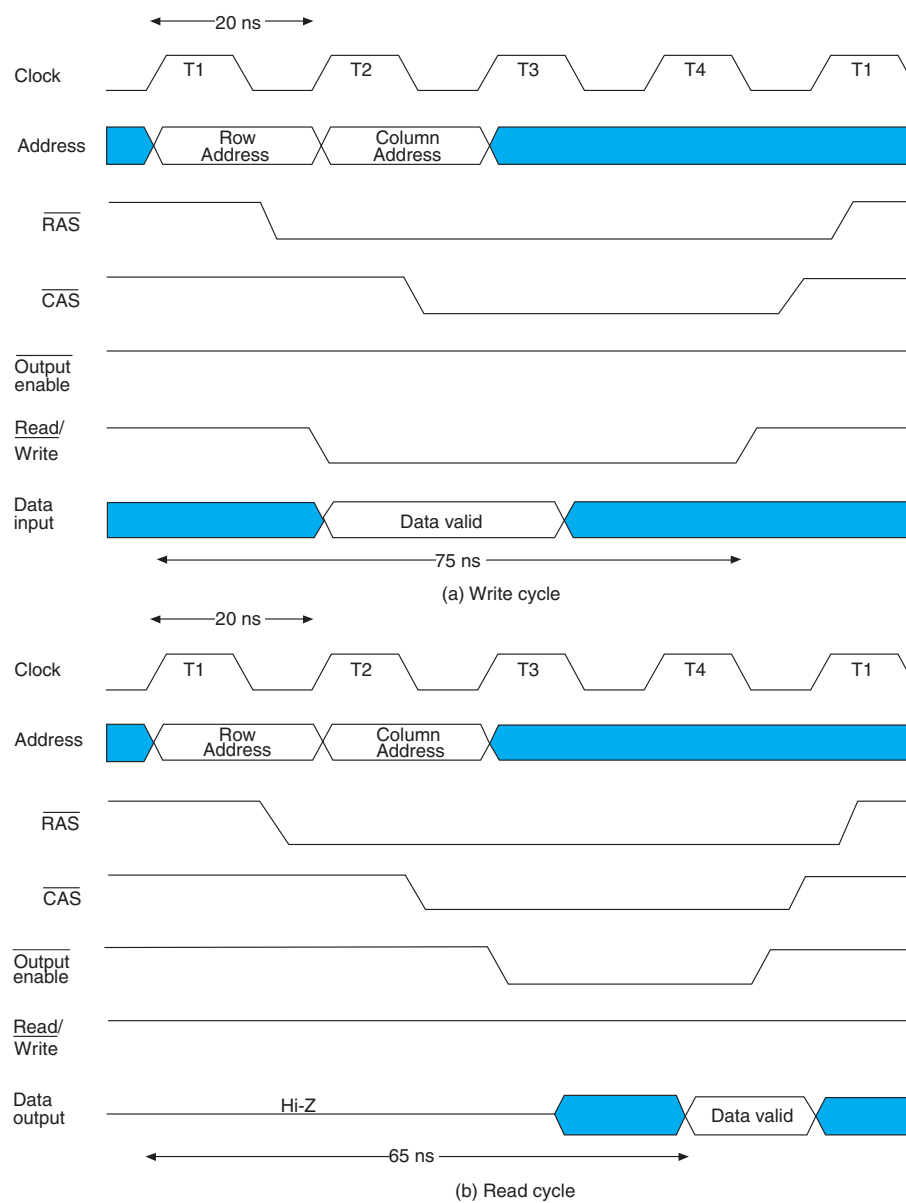


Fig. 6-15 Timing for DRAM Write and Read Operations



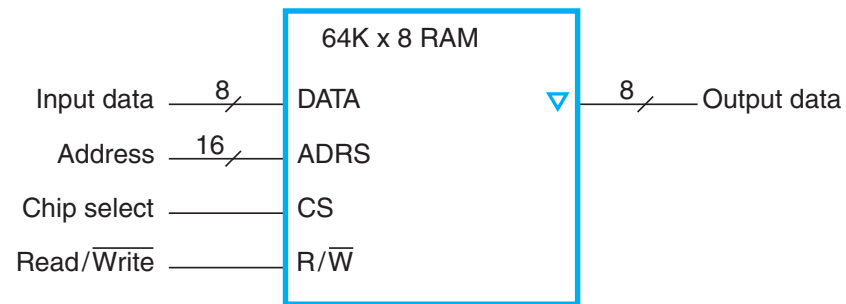


Fig. 6-16 Symbol for a 64K  $\times$  8 RAM Chip

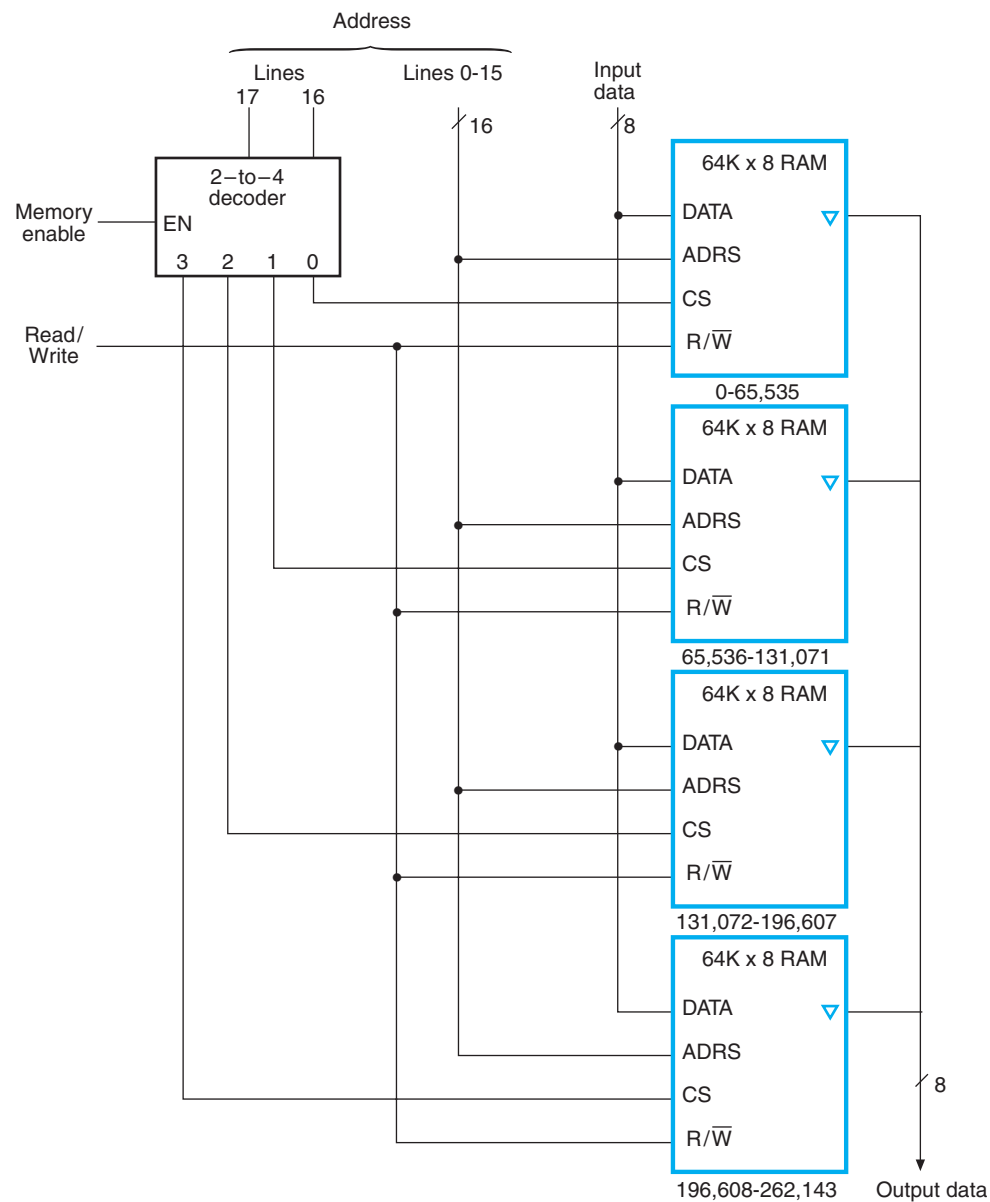


Fig. 6-17 Block Diagram of a 256K x 8 RAM

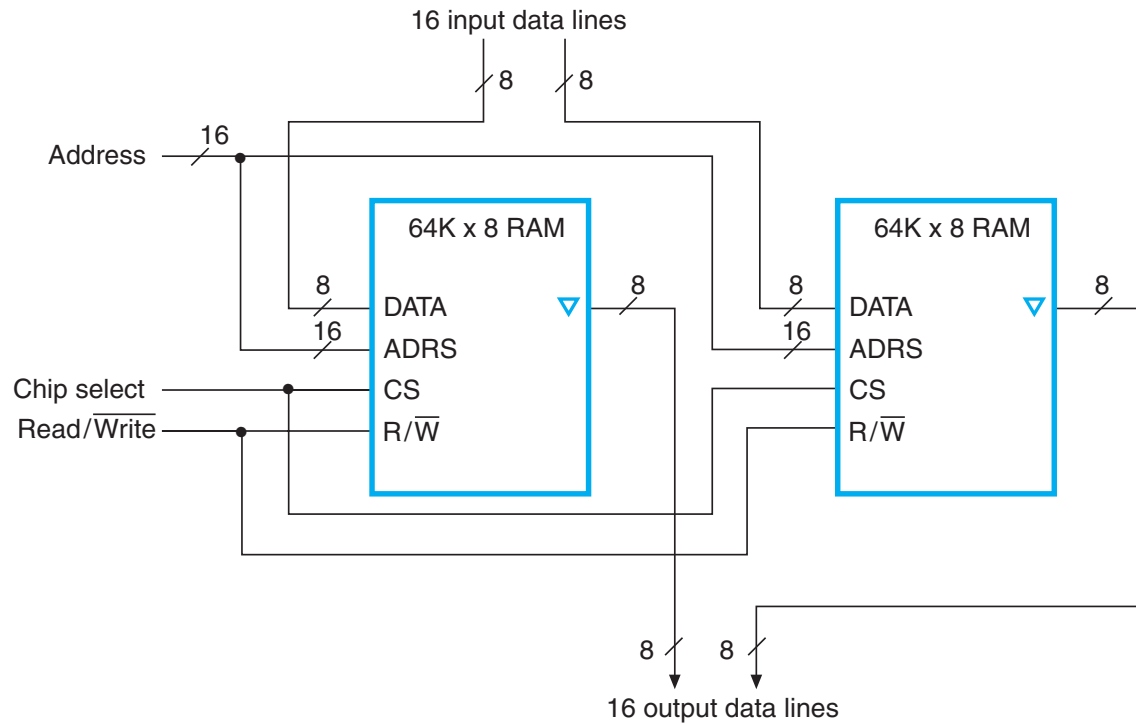


Fig. 6-18 Block Diagram of a 64K  $\times$  16 RAM

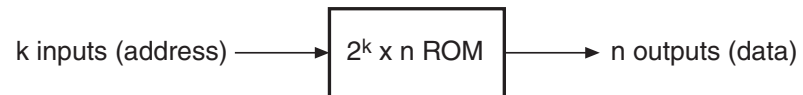


Fig. 6-19 Block Diagram of ROM

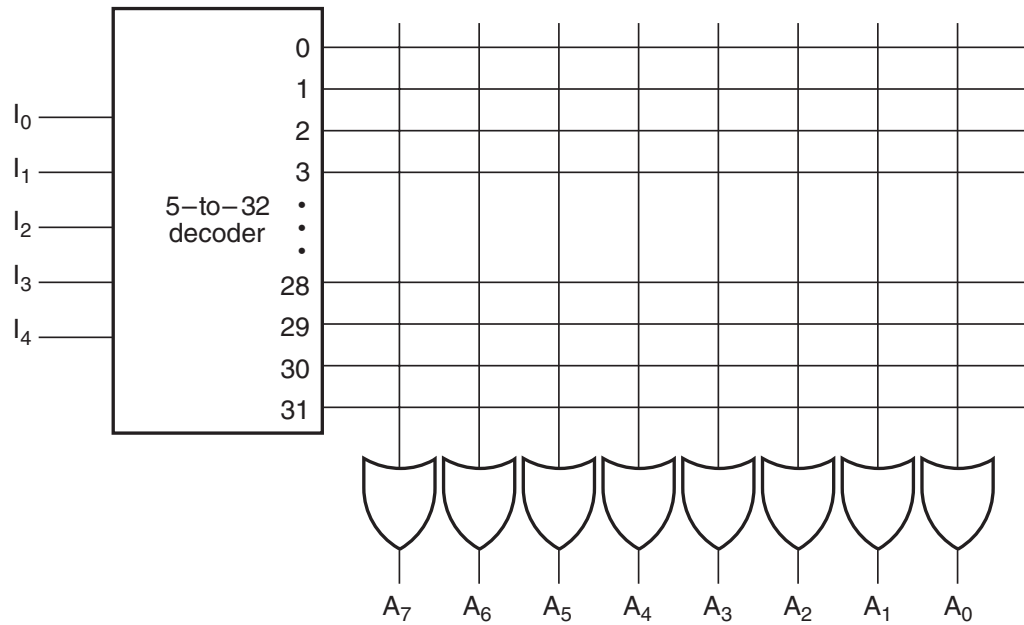


Fig. 6-20 Internal Logic of a  $32 \times 8$  ROM

**TABLE 6-2**  
**ROM Truth Table (Partial)**

Inputs					Outputs							
I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		.							.			
		.							.			
		.							.			
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Table 6-2 ROM Truth Table (Partial)

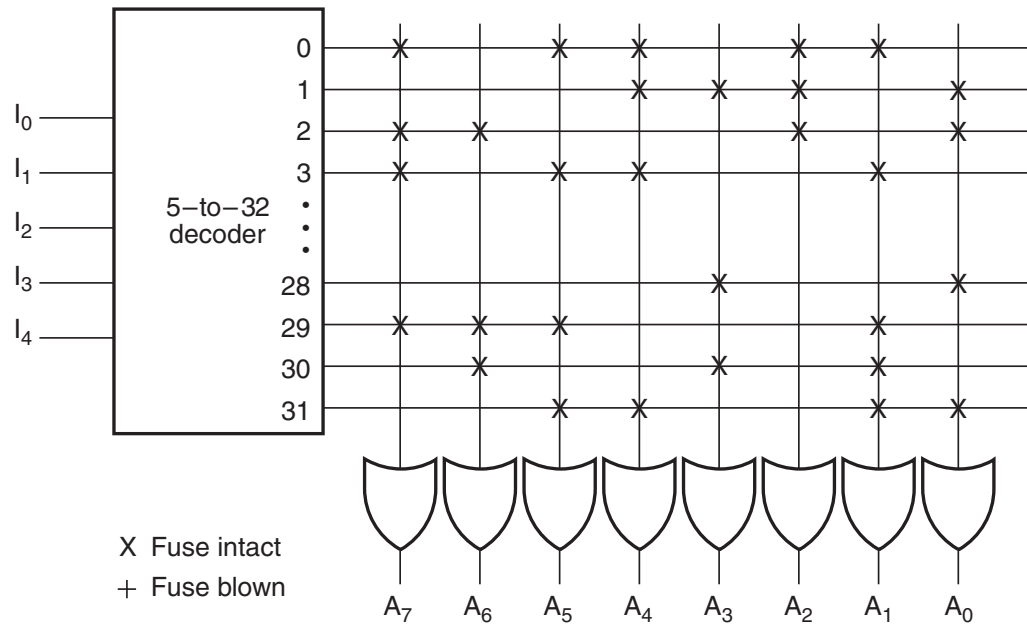


Fig. 6-21 Programming the ROM According to Table 6-2

**TABLE 6-3**  
**Truth Table for Circuit of Example 6-1**

Inputs			Outputs						Decimal
A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	B <sub>5</sub>	B <sub>4</sub>	B <sub>3</sub>	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

Table 6-3 Truth Table for Circuit of Example 6-1



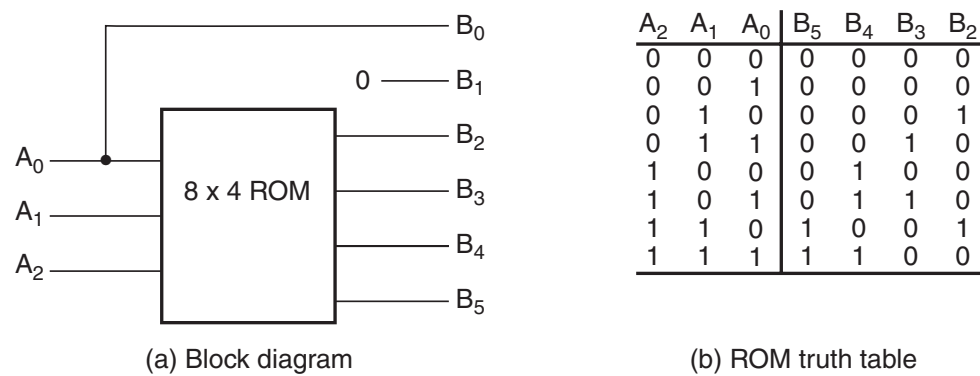


Fig. 6-22 ROM Implementation of Example 6-1

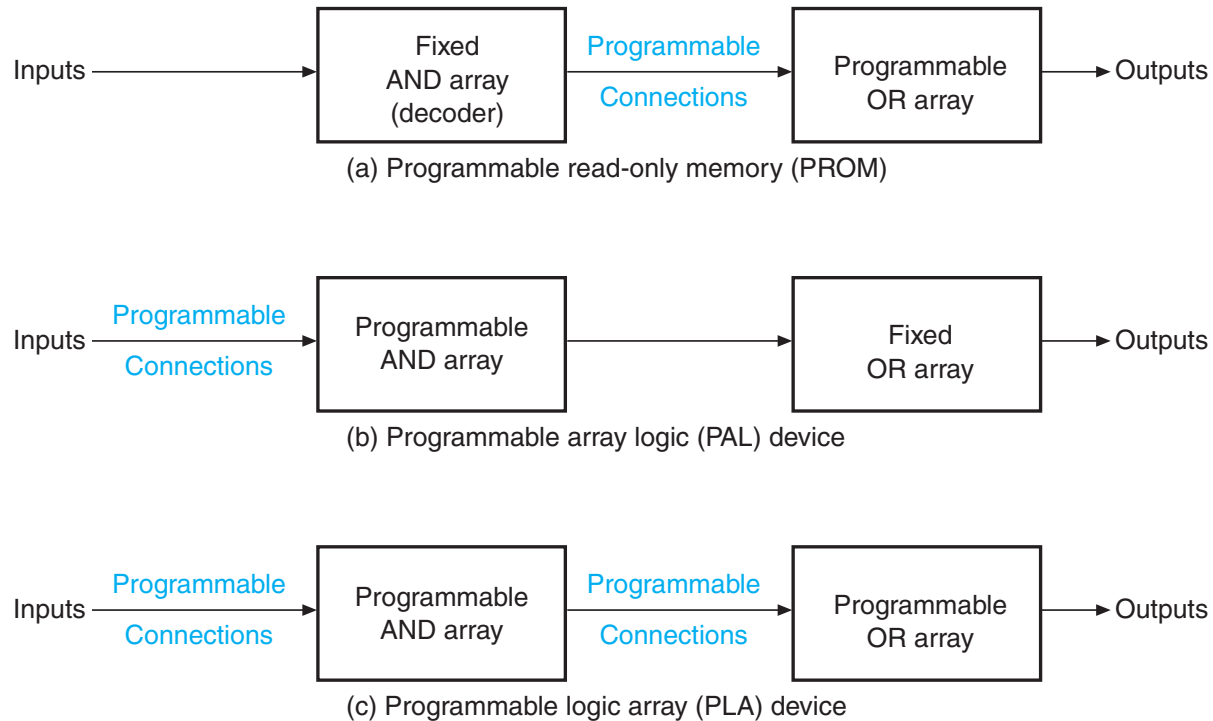


Fig. 6-23 Basic Configuration of Three PLDs

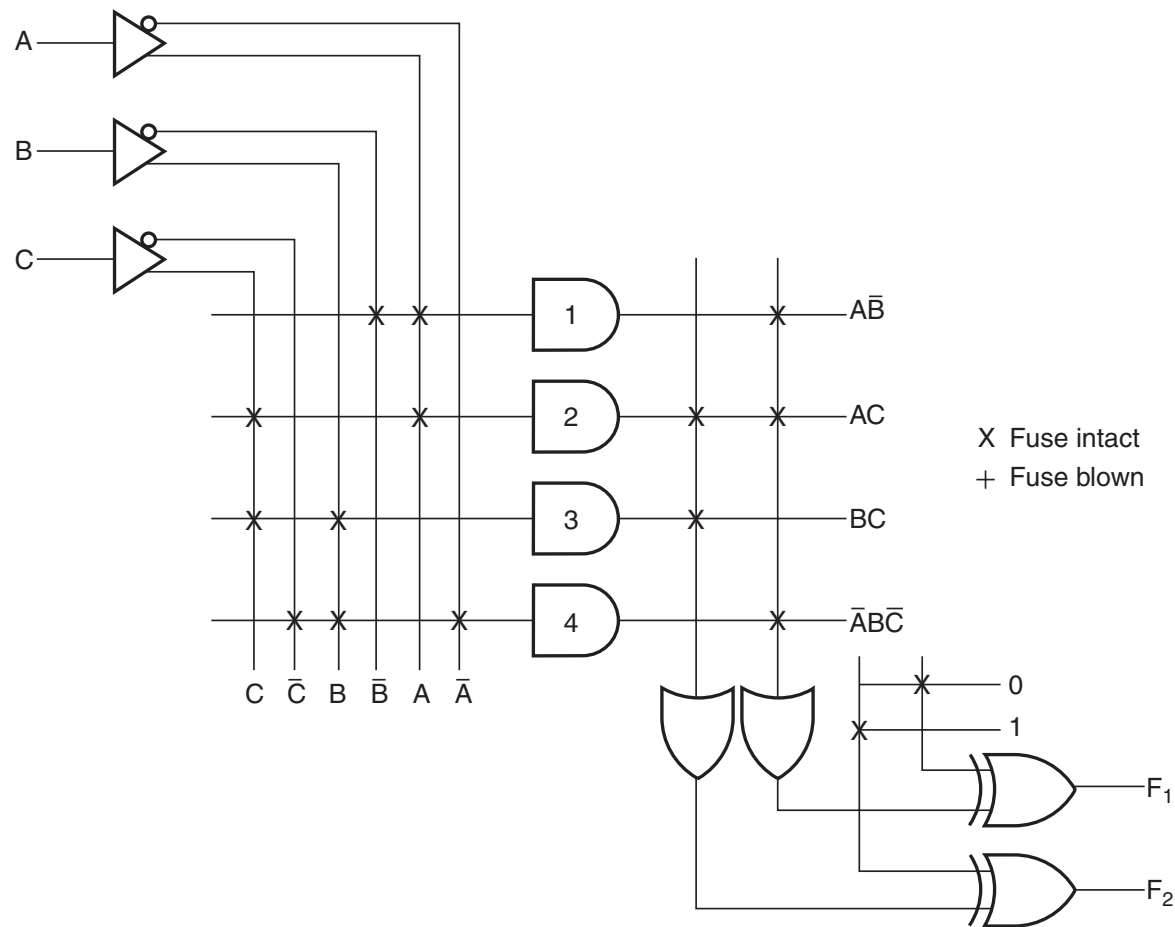
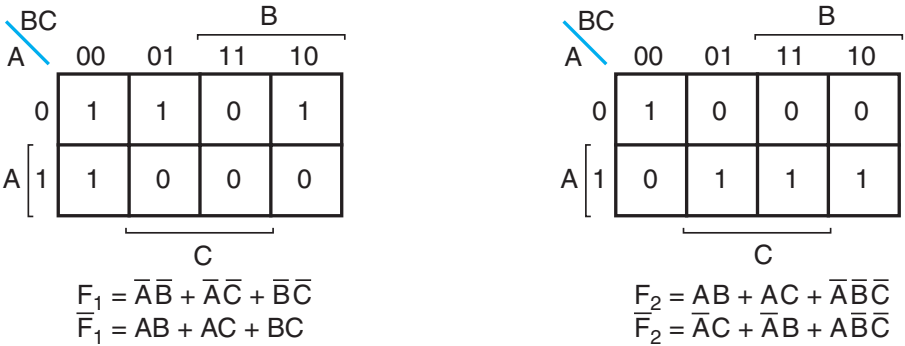


Fig. 6-24 PLA with Three Inputs, Four Product Terms, and Two Outputs

**TABLE 6-4**  
**Programming Table for the PLA in Figure 6-24**

		Inputs			Outputs	
	Product term	A	B	C	(T) F <sub>1</sub>	(C) F <sub>2</sub>
$A\overline{B}$	1	1	0	—	1	—
$AC$	2	1	—	1	1	1
$BC$	3	—	1	1	—	1
$\overline{A}B\overline{C}$	4	0	1	0	1	—

Table 6-4 Programming Table for the PLA in Figure 6-24



PLA programming table					
	Product term	Outputs			
		Inputs A B C	(C) F <sub>1</sub>	(T) F <sub>2</sub>	
AB	1	1 1 –	1	1	
AC	2	1 – 1	1	1	
BC	3	– 1 1	1	–	
$\bar{A}\bar{B}\bar{C}$	4	0 0 0	–	1	

Fig. 6-25 Solution to Example 6-2

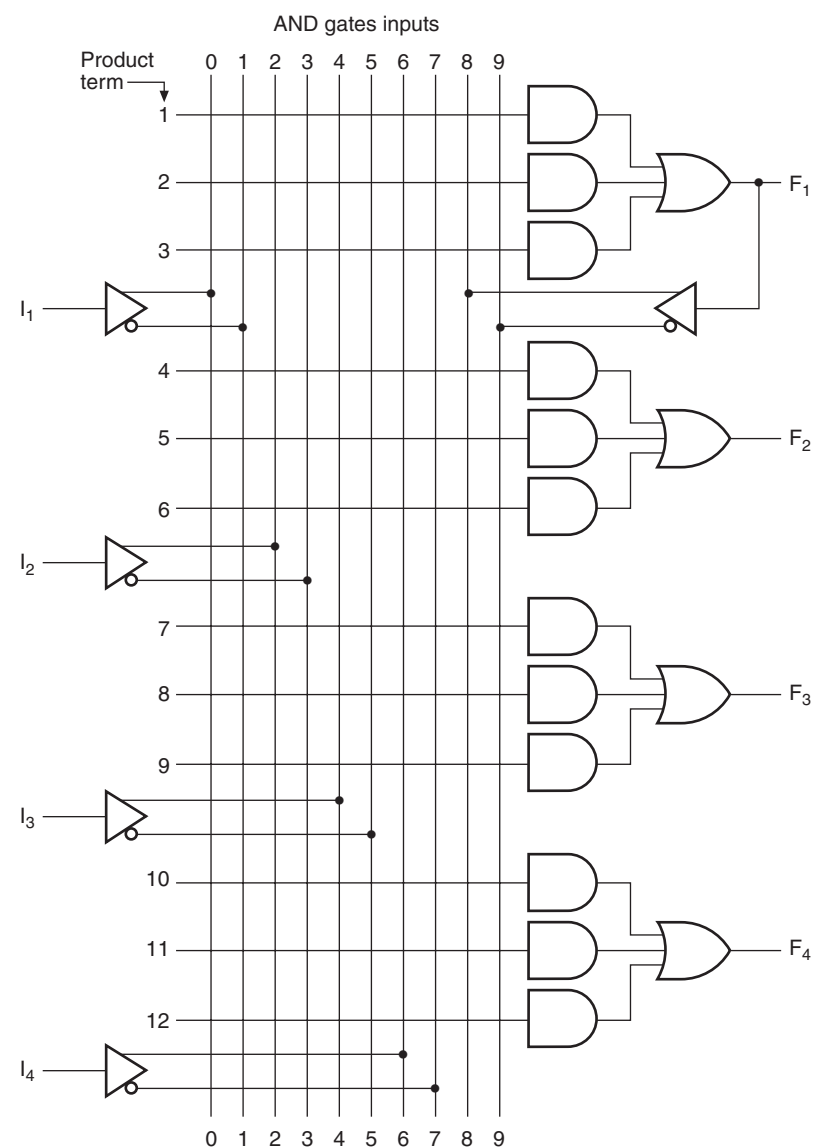


Fig. 6-26 PAL<sup>®</sup> Device with Four Inputs, Four Outputs, and a Three-wide AND-OR Structure

**TABLE 6-5**  
**PAL® Programming Table for Example 6-3**

Product term	AND Inputs					Outputs
	A	B	C	D	W	
1	1	1	0	—	—	$W = \overline{A}B\overline{C}$ $+ \overline{A}\overline{B}CD$
2	0	0	1	0	—	
3	—	—	—	—	—	
4	1	—	—	—	—	$X = A$ $+ BCD$
5	—	1	1	1	—	
6	—	—	—	—	—	
7	0	1	—	—	—	$Y = \overline{A}B$ $+ CD$ $+ \overline{B}\overline{D}$
8	—	—	1	1	—	
9	—	0	—	0	—	
10	—	—	—	—	1	$Z = W$ $+ A\overline{C}\overline{D}$ $+ \overline{A}\overline{B}\overline{C}D$
11	1	—	0	0	—	
12	0	0	0	1	—	

Table 6-5 PAL® Programming Table for Example 6-3

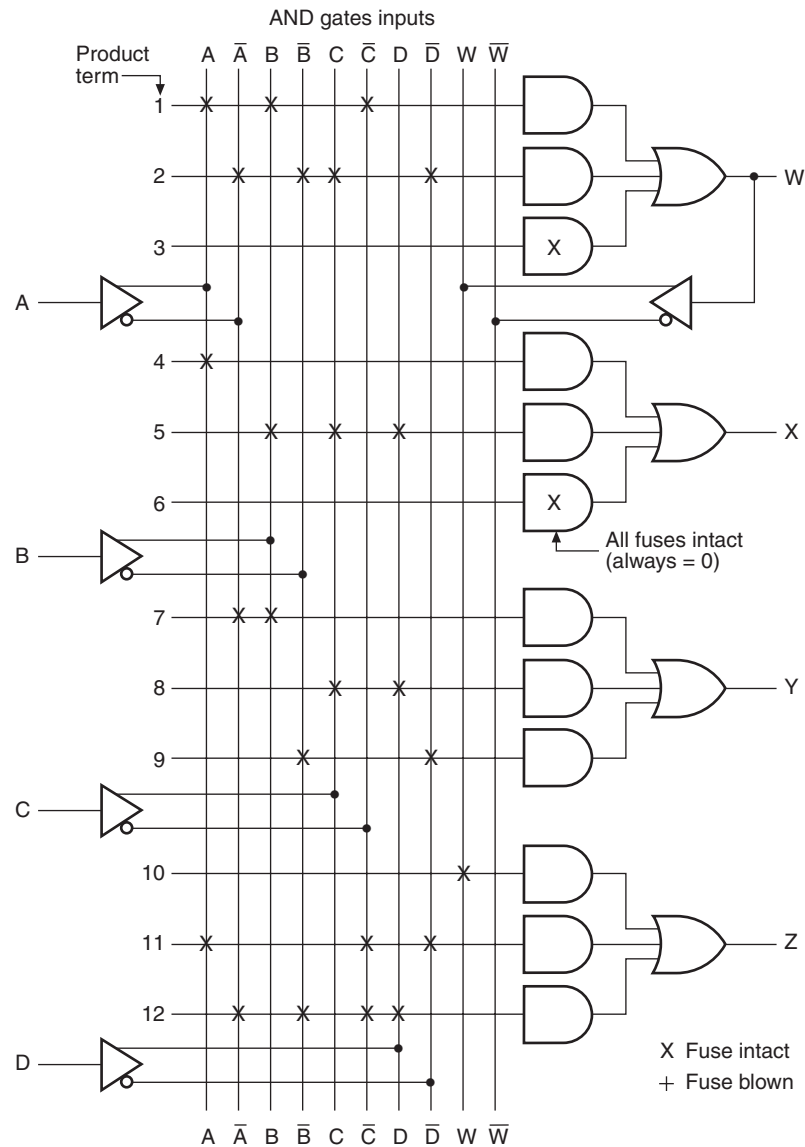


Fig. 6-27 Connection Map for PAL<sup>®</sup> Device for Example 6-3



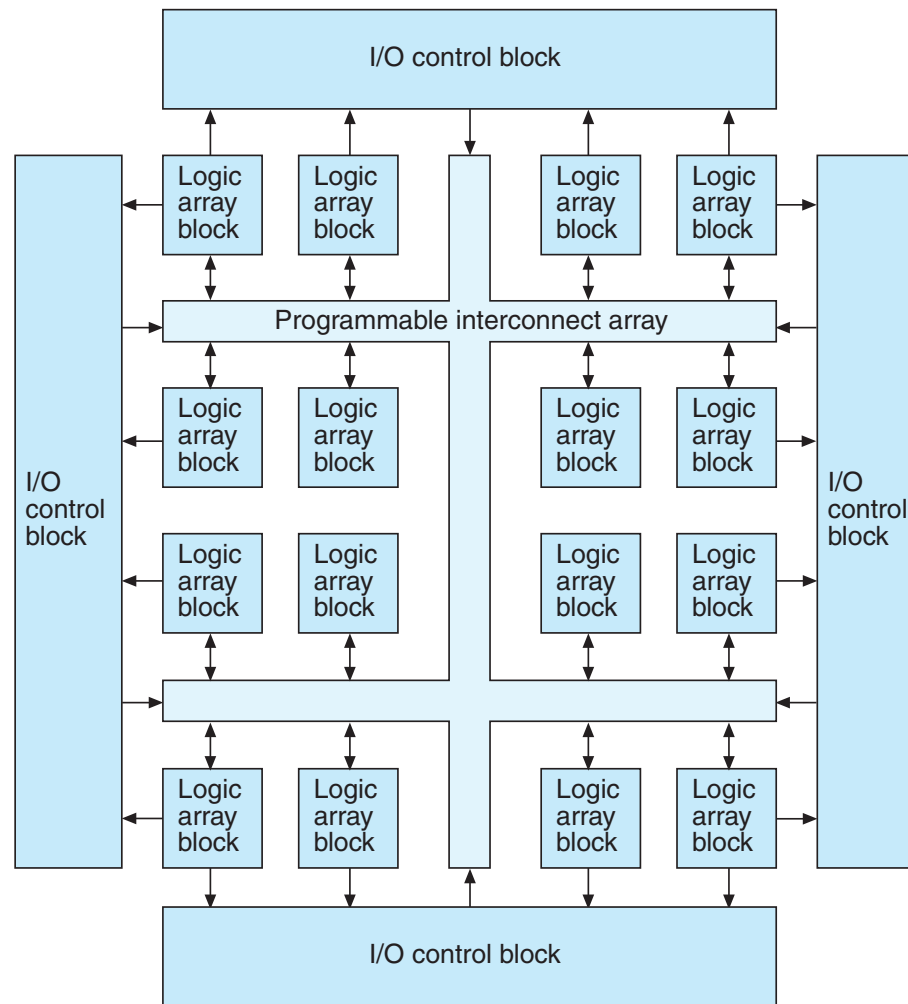


Fig. 6-28 Altera® MAX 7000™ Structure (Reprinted with Permission of Altera Corporation, © Altera Corp., 1991)

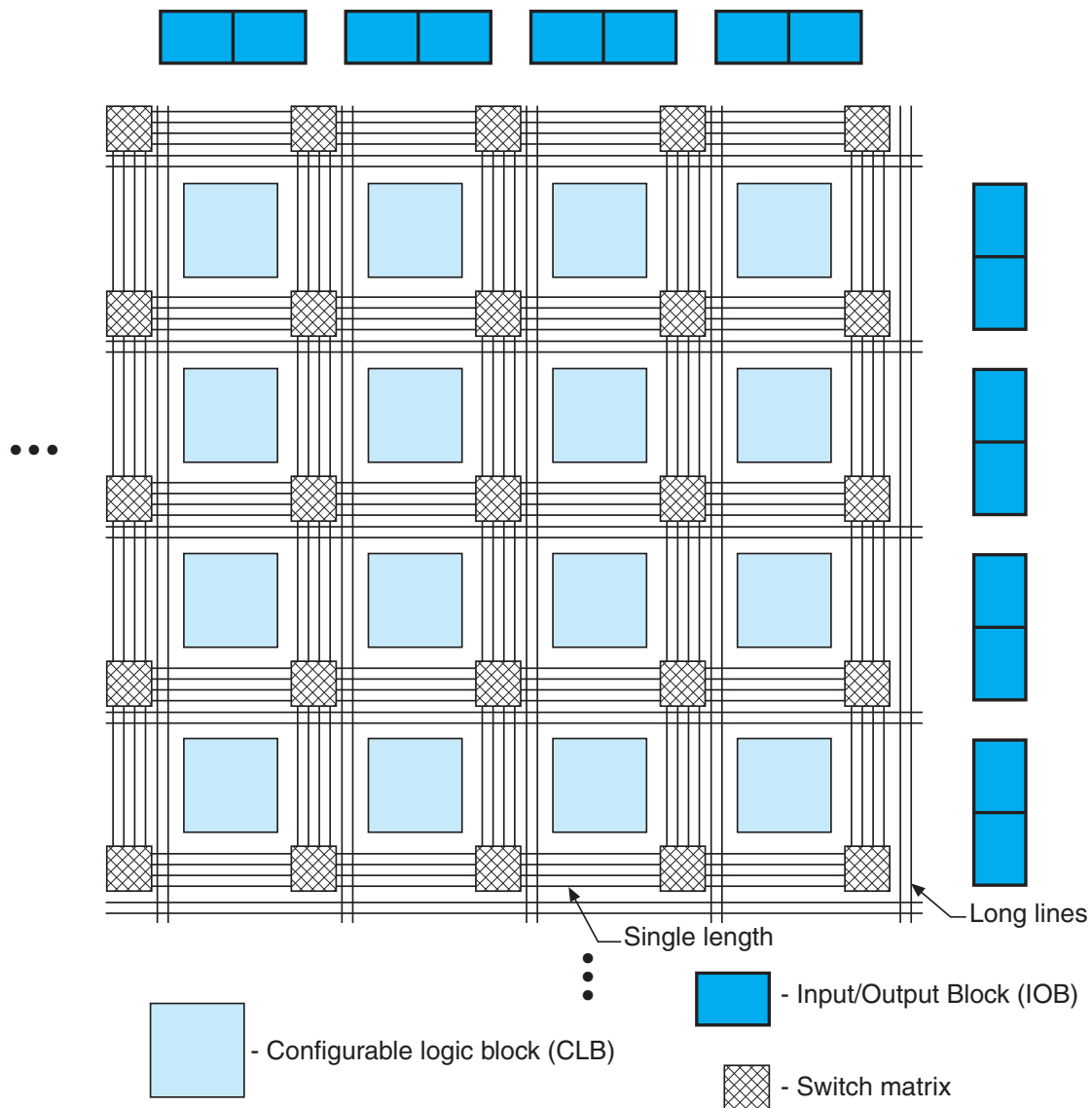


Fig. 6-29 Xilinx® XC4000™ FPGA Structure  
(Adapted with Permission of Xilinx, Inc.)

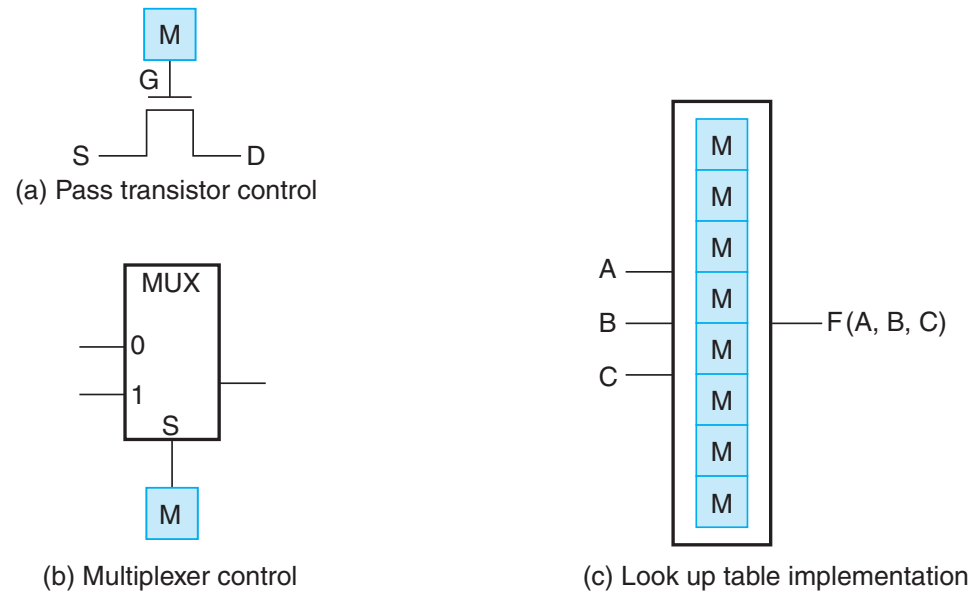
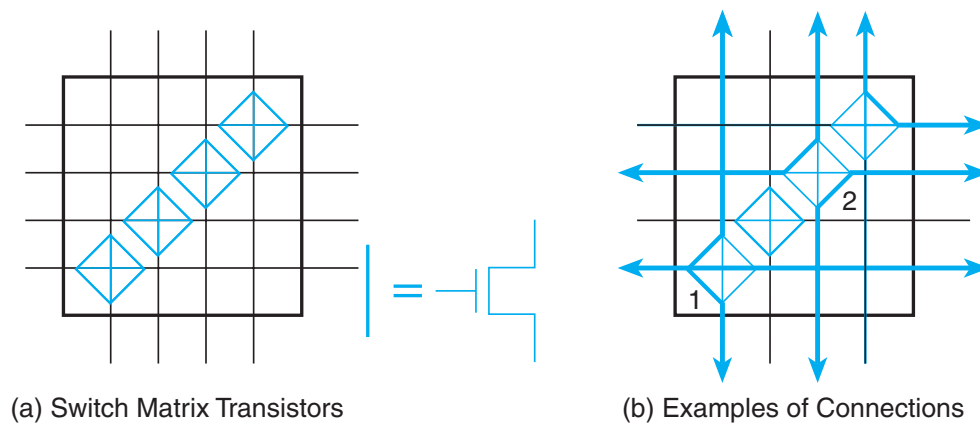


Fig. 6-30 SRAM Bit Use in Xilinx® FPGAs



(a) Switch Matrix Transistors

(b) Examples of Connections

Fig. 6-31 Example of Xilinx<sup>®</sup> Switch Matrix (Adapted with Permission of Xilinx<sup>®</sup>, Inc.)

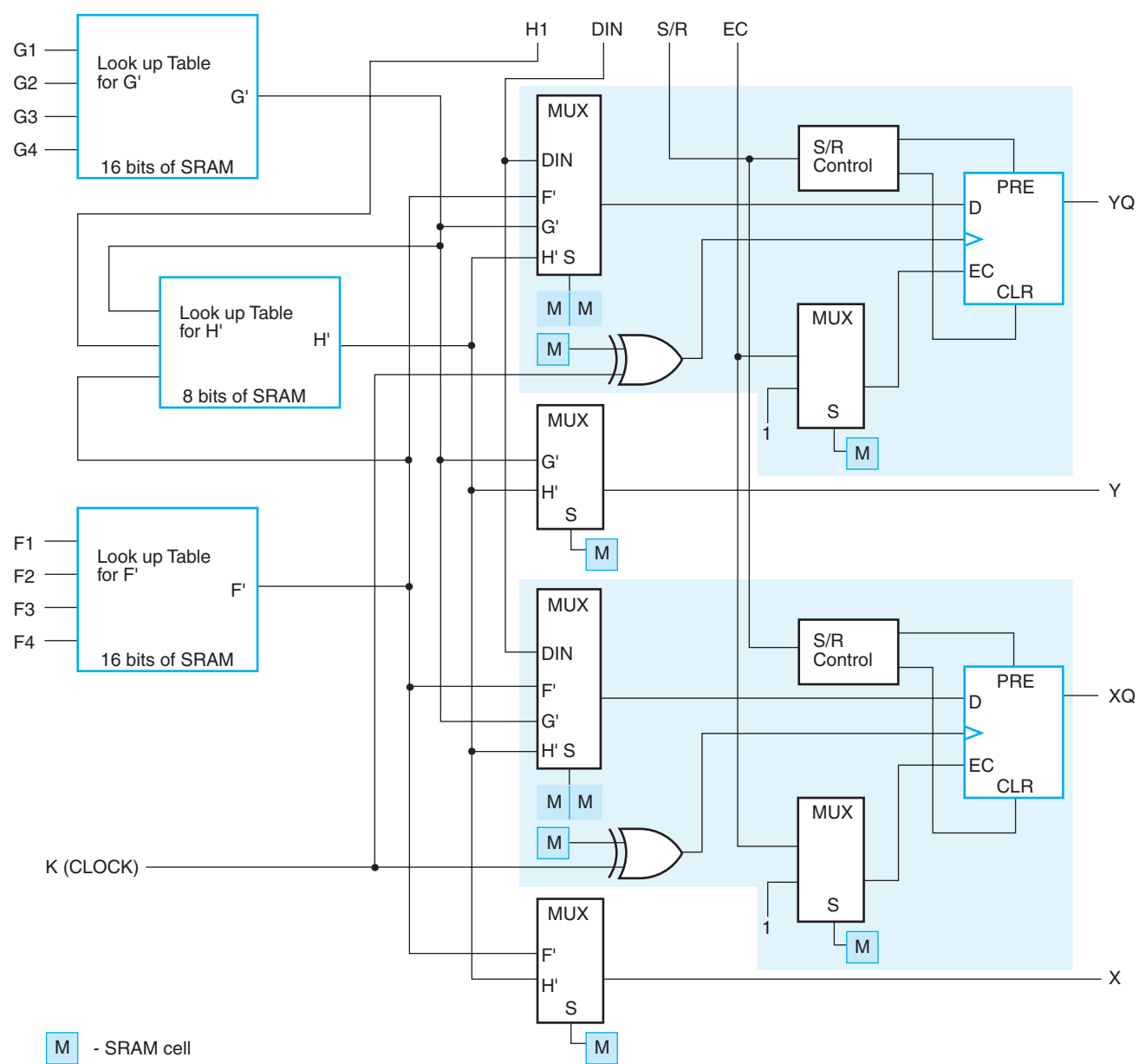


Fig. 6-32 Simplified Diagram of a Xilinx® Configurable Logic Block  
(Adapted with permission of Xilinx®, Inc.)

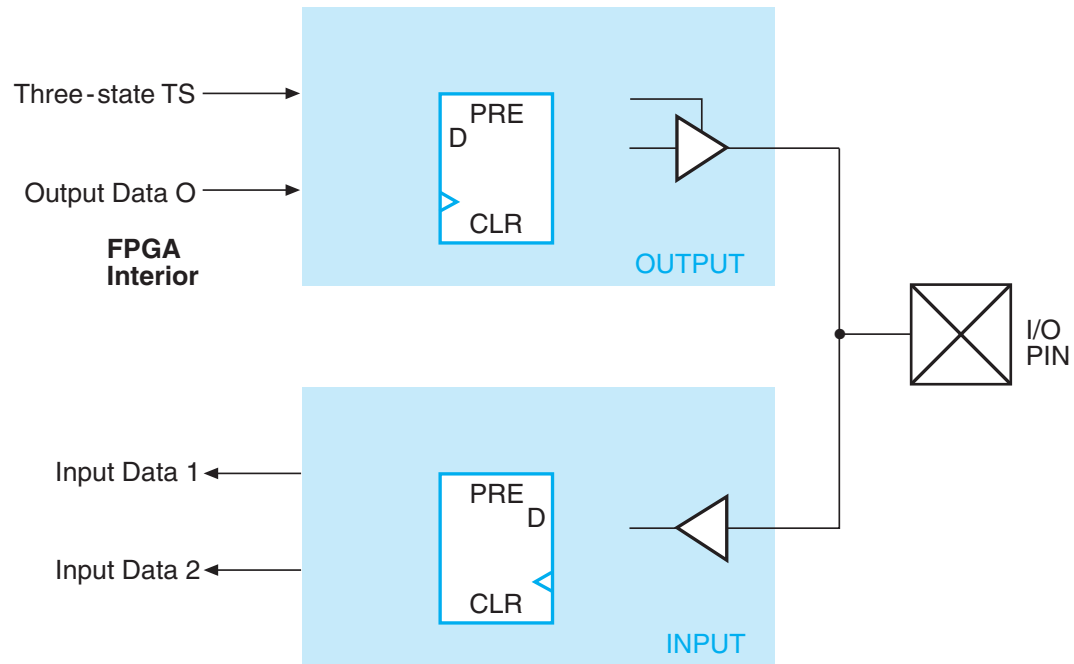


Fig. 6-33 Sketch of Xilinx<sup>®</sup> IOB Structure  
(Adapted with Permission of Xilinx<sup>®</sup>, Inc.)