# INTEGRATED CIRCUITS



Product specification File under Integrated Circuits, IC06 September 1993



## 74HC/HCT245

### FEATURES

- Octal bidirectional bus interface
- Non-inverting 3-state outputs
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

### **GENERAL DESCRIPTIONS**

The 74HC/HCT245 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT245 are octal transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The "245" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated. The "245" is similar to the "640" but has true (non-inverting) outputs.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb}$  = 25 °C;  $t_r$  =  $t_f$  = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT		
STWIDOL	FARAMETER	CONDITIONS	НС	нст		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	7	10	ns	
CI	input capacitance		3.5	3.5	pF	
C <sub>I</sub> / <sub>O</sub>	input/output capacitance		10	10	pF	
C <sub>PD</sub>	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF	

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$ 

 $f_i$  = input frequency in MHz

 $f_o = output frequency in MHz$ 

 $\sum (C_{L} \times V_{CC}^{2} \times f_{o}) = \text{sum of outputs}$ 

 $C_L$  = output load capacitance in pF

 $V_{CC}$  = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub> For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

### **ORDERING INFORMATION**

See "74HC/HCT/HCU/HCMOS Logic Package Information".

## 74HC/HCT245

### **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION					
1	DIR	direction control					
2, 3, 4, 5, 6, 7, 8, 9 A <sub>0</sub> to A <sub>7</sub>		data inputs/outputs					
10	GND	ground (0 V)					
18, 17, 16, 15, 14, 13, 12, 11	B <sub>0</sub> to B <sub>7</sub>	data inputs/outputs					
19	OE	output enable input (active LOW)					
20	V <sub>CC</sub>	positive supply voltage					



## 74HC/HCT245



### FUNCTION TABLE

INP	UTS	INPUTS/OUTPUTS					
OE	DIR	A <sub>n</sub>	B <sub>n</sub>				
L	L	A = B	inputs				
L	н	inputs	B = A				
Н	Х	Z	Z				

#### Notes

1. H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

## 74HC/HCT245

### DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver  $I_{CC}$  category: MSI

### AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
SYMBOL		74HC									WAVEFORMS
STIVIBOL		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORWIS
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t <sub>PZH</sub> / t <sub>PZL</sub>	$\begin{array}{l} 3 \text{-state output enable time} \\ \hline \overline{OE} \text{ to } A_{n;} \\ \hline \overline{OE} \text{ to } B_n \\ signalname \text{ DIR} \end{array}$		30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PHZ</sub> / t <sub>PLZ</sub>	$\begin{array}{l} \mbox{3-state output disable time} \\ \hline \overline{OE} \mbox{ to } A_{n;} \\ \hline \overline{OE} \mbox{ to } B_n \\ \mbox{signalname DIR} \end{array}$		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

## 74HC/HCT245

#### DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: bus driver  $I_{CC}$  category: MSI

#### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT						
A <sub>n</sub>	0.40						
B <sub>n</sub> OE	0.40						
OE	1.50						
DIR	0.90						

#### AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS		
		74HCT									WAVEFORMS	
		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(,,,		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n;</sub> B <sub>n</sub> to A <sub>n</sub>		12	22		28		33	ns	4.5	Fig.5	
t <sub>PZH</sub> / t <sub>PZL</sub>	$\begin{array}{l} 3\text{-state output enable time} \\ \hline \overline{OE} \text{ to } A_{n;} \\ \hline \overline{OE} \text{ to } B_n \\ signalname DIR \end{array}$		16	30		38		45	ns	4.5	Fig.6	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	$\begin{array}{c} 3\text{-state output disable time} \\ \hline \overline{OE} \text{ to } A_{n;} \\ \hline \overline{OE} \text{ to } B_n \\ signalname DIR \end{array}$		16	30		38		45	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5	

## 74HC/HCT245

### AC WAVEFORMS





### PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".