Metrology Roadmap: A Supplement to the National Technology Roadmap for Semiconductors

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Abstract: The Metrology Roadmap is a supplement to the National Technology Roadmap for Semiconductors. The off-line, in-line, and in-situ analysis requirements for development and manufacture of silicon integrated circuits are presented in a form that facilitates direct reference to the roadmap. The Metrology Roadmap is divided into the following sections: Introduction; Sensors and Methodology for In-Situ Process Control; Process Integration, Devices & Structures; Materials and Bulk Processes; Lithography; Interconnect; Factory Integration; and Measurement Capability. Representatives from SEMATECH member companies (Analytical Laboratory Manager Working Group), National Institute of Standards and Technology (NIST), National Laboratories such as SANDIA, and suppliers involved in development and routine use of off-line, in-line, and in-situ metrology tools developed this roadmap using the process and materials requirements taken from the roadmap.

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INTRODUCTION

METROLOGY — A PARADIGM SHIFT

The timely achievement of evolving requirements of the National Technology Roadmap for Semiconductors (NTRS) requires a paradigm shift in the role of metrology from off-line sampling to on-line control. The most important enabler for the shift is the realization by management executives that metrology tools must transition to the same level of robustness and hence development support as is accorded to process equipment. A key to establishing this new paradigm is combining the use of in situ and in-line metrology with off-line capabilities for advanced process control and rapid yield learning.

National Institute of Standards and Technology, (NIST), Semiconductor Research Corporation (SRC), SEMATECH, American Society for Testing and Materials (ASTM), Semiconductor Equipment and Materials, Int'l. (SEMI), metrology tool suppliers, and the national laboratory and university community need to cooperate on standardization of methods and production of reference materials and improved measurement methods. The National Semiconductor Metrology Program already established at NIST has this cooperation as one objective, and completion of funding of the Program must be vigorously pursued. Existing national laboratory project activities should be coordinated with the NIST metrology program.

The lack of statistical methodologies hampers process control metrology. The impact of infrequent events on yield is well known, and the metrology tools must be accompanied by statistically sound sampling, testing, and correlation with physical parameters. Statistical methods associated with detection limits, non-normal data, and distributional data must be developed.

CONTENTS AND SCOPE

The scope of the Metrology Roadmap is to summarize the off-line, in-line, and in situ physical analysis requirements associated with the NTRS document. In order to facilitate reference to the NTRS, the Metrology Roadmap employs the same general format as the NTRS. Therefore, the Metrology Roadmap projects these needs for the next 15 years, according first volume shipment of a generation of DRAM technology. First shipment of DRAMs having 0.25 μm design rule features will be in 1998. The roadmap contains measurement requirements taken from the NTRS, indicates the challenge to existing technology, and indicates consensus potential solutions when appropriate. For each area, the current technology status, needs, and potential solutions are discussed and a combination needs, existing technology, and potential solutions roadmap are provided. While many metrology needs are shared by all areas of the NTRS, this booklet categorizes metrology needs in an identical manner to the NTRS. For example, the process requirements for metallic contamination levels is listed in the Starting Materials and Wafer Surface Preparation subsections of the Materials and Bulk Processes section. The only exception is the chapter on Sensors and Methodology for In-line Process Control. In order to emphasize the paradigm shift in metrology toward process control, this area was given special attention. The final section is a short discussion on measurement capability analysis. This is a critical section that applies to all areas of metrology.

Future roadmaps need to include Packaging Metrology and Electrical Test Metrology Needs.

CAPITAL PRODUCTIVITY AND COST OF OWNERSHIP

In conjunction with the paradigm shift moving metrology to a more in-line and in situ operations are the requirement for robust tools and methods and the increased awareness of cost of ownership and its impact on cost/resource for the entire manufacturing facility. Existing cost of ownership models are primarily aimed at in-line process tools and fab facilities. SEMATECH has applied this methodology to optical particle detection systems and SEM/EDX whole wafer defect review tools. There is a clear need for expanding this methodology to in situ, other in-line, and off-line methods. Since clean room space is costly when compared to laboratory-based systems, metrology tools were not given a high priority. A new emphasis on metrology requires a new methodology for comprehending the true value of development, pilot line, and production fab metrology. The contribution of metrology to rapid yield learning requires factory-wide data analysis and management systems. These systems must be comprehended in cost/resource models.

ROADMAPPING PROCESS AND ACKNOWLEDGEMENTS

The Metrology Roadmap is a consensus document that was compiled using the inputs of several groups including: the Analytical Laboratory Managers Working Group, the Metrology group of Silicon Council, and the Metals Task Force of the Silicon Council, suppliers of analytical equipment. The Materials and Bulk Processes Technical Working Group (MBP-TWG) added a Metrology discussion to the MBP section of the National Technology Roadmap for Semiconductors, and the inputs of the entire MBP-TWG were very important to the development of this roadmap. At the MBP-TWG meetings, Jim Greed provided insights from the SEMI community, and Dave Seiler provided inputs from NIST. The Materials and Bulk Processes Metrology Workshop held May 5 and 6, 1994 further developed key sections of this roadmap. The in situ process control section was developed by Gary Rubloff, Jimmy Hosch, and Bob Scace at the MBP Metrology Workshop. The Lithography Metrology section in this document was championed and developed at the Lithography Metrology Workshop by Robert Hershey. The Interconnect section was based on inputs from Ken Maxwell, Ken Monnig, Rex Wright, and the Plasma Diagnostics Workshop. A list of participants can be found on pages v to ix.

SENSORS AND METHODOLOGY FOR IN SITU PROCESS CONTROL

This section covers general requirements for process control sensors including the associated methodology. Process control sensors are divided into the categories of equipment state, process state, and wafer state. Process control methodology categories include: equipment/process model/design, fault detect/classification, and adaptive process control. At each stage of deployment, process control implementation should be strategically utilized to improve the timeliness of yield learning.

COMMENTS AND PRIORITIES

- All process control is model based.
- Sensors shorten learning time feedback loop.
- Run-to-run control and process state sensors are the highest priority for in situ sensors.
- Migrate to real-time control except for high priority items such as rapid thermal processing (RTP) temperature control needs.
- Migrate wafer state to in situ from in-line in evolutionary way.

BACKGROUND

The fundamental work in process and tool modeling will drive process control strategies. Process models allow selection of relevant physical parameters for control of microfeature and wafer-level process such as tungsten via filling. Control software for local tool control must evolve to the factory level. Contamination control sensors and process control will follow similar paths.

CURRENT TECHNOLOGY STATUS

Metrology is used mostly off-line, to some degree in-line, and rarely in situ to develop and control IC manufacturing processes and starting materials. Metrology needs to move from off-line to in-line and in-line to in situ process control. Prevention of process excursions by process control sensors should significantly reduce product loss. Models and standards required for process control are under development. Existing sensors can already be applied to many of the near-term requirements. Cost of ownership models that suggest how to apply sensors and in-/off- line analysis must be developed to guide sensor and process control model development and application.

NEEDS ROADMAP

When possible, in-line or in situ non-destructive analysis of product wafers is preferable. A strategy for real time process methodology is required for cost effective implementation. In Figure 1 potential solutions for sensors and methodology for process control are presented. Equipment state sensors monitor mechanical and electrical status. Equipment state information will move from local tool to global control as connections to the CIM framework are developed. Process state sensors monitor chemical/physical parameters, temperature, and spatial distribution, and process models allowing control will be developed and improved. Wafer state sensors will monitor product parameters and uniformity. Process control methodology will require significant development if real time control is to be achieved. Development of cost of ownership models is another critical need.

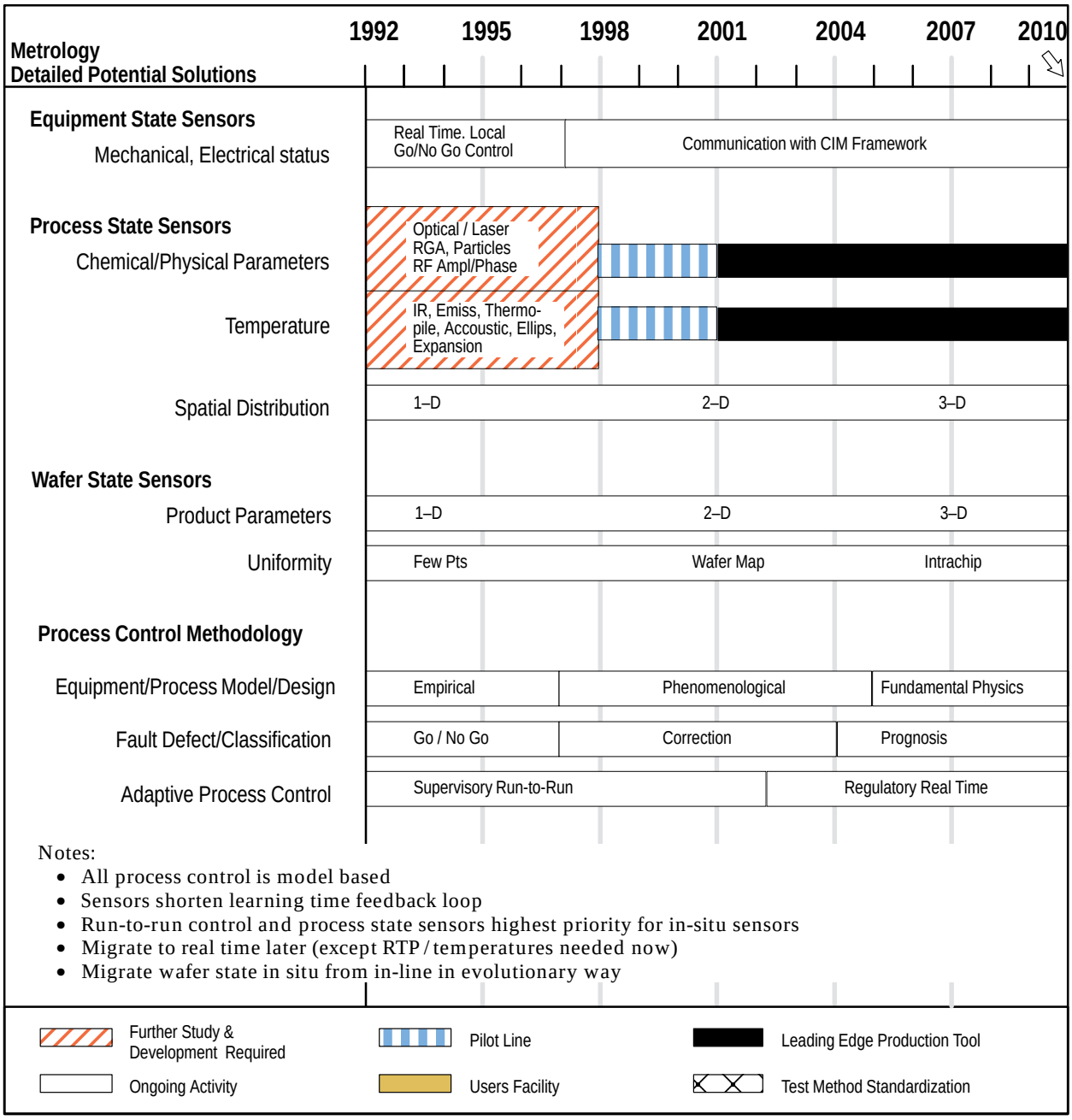


Figure 1 In Situ Process Sensors/Control

Figure 1 Note:

The following description is a generalized view of the potential solutions for achieving real time process control. Process control sensors can be categorized into equipment state, process state, and wafers state sensors. Currently, equipment state sensors provide Go/No Go control at the process tool. Some equipment state sensors provide real time control. The local control is expected to migrate toward a more global control through the CIM framework. Process state sensors are used to control chemical/physical parameters (such as moisture in vacuum, particles in a plasma, the plasma, etc.) and temperature. These sensors must provide real time control and evolve toward a capability to control processes in three dimensions. Wafer state sensors are preferable to other types of sensors, but usually not available. One example of a possible in situ sensor for control of etch process is critical dimension measurement by scatterometry. Wafer state sensors are expected to migrate toward more detailed mapping (few points on a wafer to intrachip) and develop capabilities that not only work in the presence of topographical features, but control process in high aspect ratio structures. As mentioned in the text, all process control is model based. This model refers to software that incorporates a physical basis of the process model and an action based on the information observed during processing. The control models are expected to develop the capability to regulate the process in real time and predict the viability (parametric and yield predictions) of the product wafers being processed and those in the process que.

PROCESS INTEGRATION, DEVICES & STRUCTURES

The scope of the Process Integration, Devices & Structures roadmap includes overall technology characteristics, a discussion of the current status of current memory and high performance logic technologies, technology computer aided design TCAD, and future needs for memory and logic. The discussion includes key issues for strategic employment of metrology such as short flow methodologies, known good die, yield analysis and defect allocation strategy, reliability characterization, and models for devices and structures. One example is the discussion of known good die, which refers to a die that has been shown to have the same quality standards as it would have in the fully packaged form. This type of electrical qualification of the bare die places requirements on the test equipment. Similarly, the effective use of physical metrology tools in pilot line FABs must comprehend short-loop methodology. The use of standardized test structures for short-loop tool and process development is an issue discussed in the process integration and other sections of the roadmap. The term "statistical metrology" is used to describe a fundamental method of short flow equipment characterization that can isolate the statistically significant variation of process tool output. Due to the infrequent nature of tool-induced failures, "Statistical Metrology" is based on electrical testing. In this document, we discuss the need for statistically significant sampling for physical metrology tools (see introduction) for all stages of development and for manufacturing. In both cases, the intent is to reduce the learning cycle time and allow high yield manufacturing.

COMMENTS AND PRIORITIES

Only one physical metrology need is given a priority, and it is mentioned in the table on TCAD Top Priority Needs. It is ranked and listed as follows:

4) Two/three dimensional doping profile measurement tools.

NEEDS

A number of physical characterization needs were discussed in the unpublished TCAD characterization roadmap. These include two/three dimensional defect and dopant profiles and imaging for very small features, along with quick, inexpensive imaging methods for measurement of features across die and wafer. The consensus version of the potential solutions for two/three dimension dopant and defect profiling follows (Figure 2).

Developments in the area of process integration, devices, and structures will require the evolution of several existing analysis tools. One example is the automation improvements predicted for the whole wafer FIB (focused ion beam analysis tool). "Dual Column" FIBs are now equipped with SEM/EDX capability and precision sample stages that accept defect detection tool coordinates and software that drives to specific locations in a CAD circuit layout. "Rewiring" pilot line ICs can be done using a FIB equipped with a metal halide gas source. Process integration and rapid yield learning will also require the integrated data management systems for sensors and metrology tools. These systems are discussed in the Factory Integration section of this document.

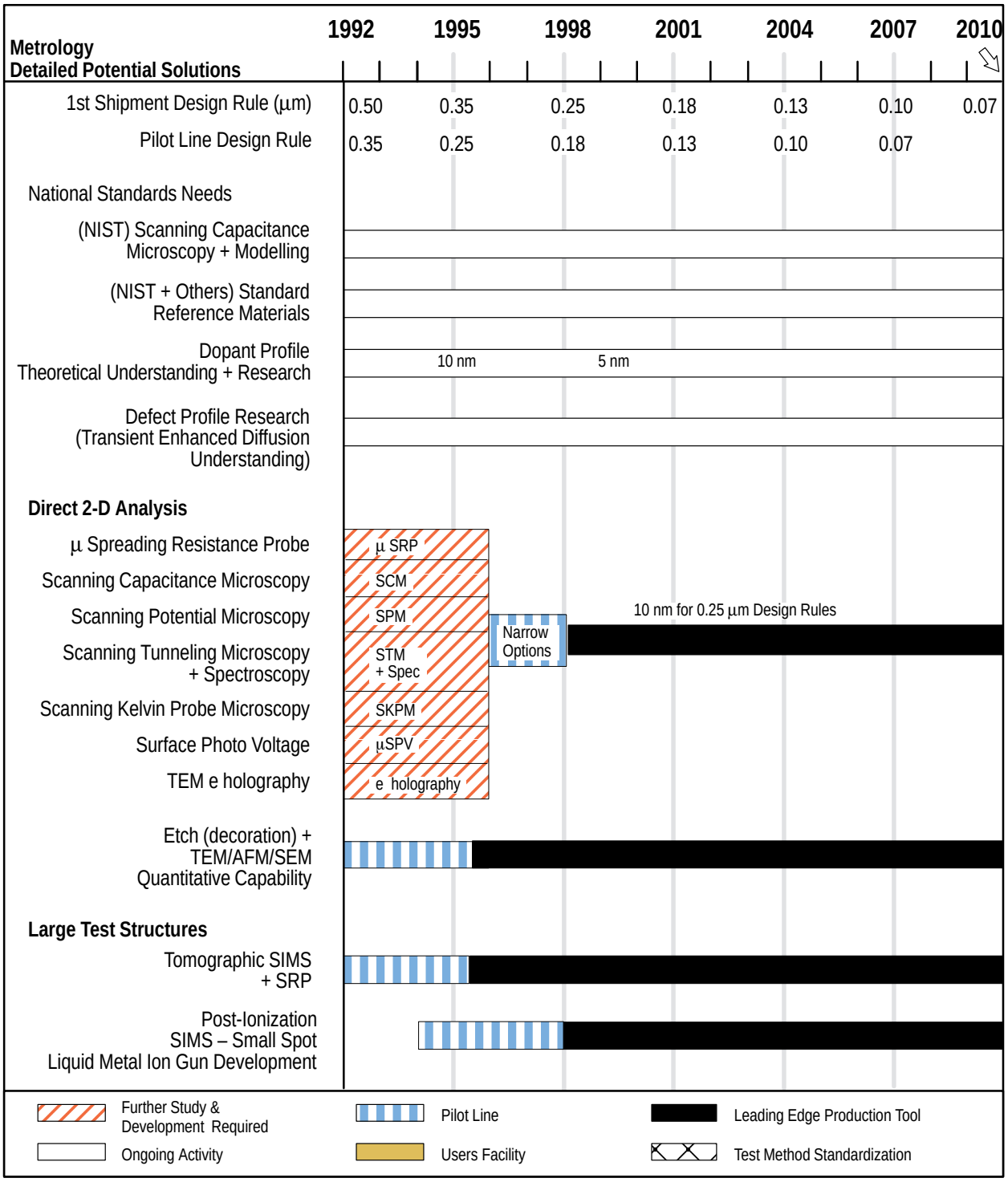


Figure 2 TCAD + Materials and Bulk Processes 2-D Profiling Metrology

Figure 2 Note:

This figure details NIST project work, research needs, and physical methods for characterizing 2 and 3 dimensional dopant profiles. The scanning capacitance microscopy and standards work are expected to continue at NIST. A clear consensus exists for the need for a theoretical understanding of experimental dopant profile data and basic research into defect profiles. There are a variety of approaches to calibrating process simulators. The activity in this area can be described as direct 2-dimensional analysis of transistors or analysis of large test structures. Since 2-D dopant profiling is not expected to be done in a FAB, the Pilot Line symbol refers to beta site tools.

MATERIALS AND BULK PROCESSES METROLOGY

Materials and Bulk Process (MBP) section of the NTRS is divided into Starting Materials, Wafer Surface Preparation, Doping Technologies, Thermal/Thin Film Processing, and Contamination Free Manufacturing (CFM). The CFM section for the entire NTRS was placed in the MBP section. A number of metrology needs span several sections of the MBP roadmap and sections of other roadmaps such as contamination analysis for Interconnects.

CURRENT TECHNOLOGY STATUS

Metrology is used mostly off-line, to some degree in-line, and rarely in situ to develop and control IC manufacturing processes and starting materials. Standard electrical test procedures for gate dielectrics is the highest priority need for Materials and Bulk Processes. These test procedures will foster both process and gate dielectric tool development. The lack of standard methods and reference materials for analysis of metallic and organic contamination is impeding cost-effective process development for surface preparation and starting materials.

COMMENTS AND PRIORITIES

Each section of the MBP roadmap listed priorities for unique metrology needs that are unique to that section. These are listed below.

STARTING MATERIALS

- Metrology tools to handle 300 mm wafers
- Standard methods and reference materials for recombination/generation carrier lifetime measurements.
- Novel mapping/non-destructive in-line carrier lifetime correlation with metallic and structural defects.
- Reference materials for metallic contamination

SURFACE PREPARATION

- Real time, in situ sensors for chemical, contaminants, and dissolved gases.

DOPING TECHNOLOGIES

- Charge monitor wafers
- Junction Leakage wafers
- SOI Characterization
- Shallow Junction SIMS and SRP Profiling

THERMAL/THIN FILMS

- Standard Electrical Test Procedures for Gate Dielectrics
- Temperature Measurement for Rapid Thermal Processing
- Thin Film Thickness Measurement

CONTAMINATION FREE MANUFACTURING

- Particle Reference Materials

NEEDS ROADMAP

When possible, in-line or in situ non-destructive analysis of product wafers is preferable. A strategy for real-time process methodology is required for cost effective implementation. In Figure 1, potential solutions for sensors and methodology for process control are presented. Major gaps in in-line and off-line capabilities include:

- Data management systems that are an integral part of process control, defect detection and sensors, and data reduction methods
- Standard reference materials and methods for all areas of metrology
- Improved metrology for particle identification, metallic and organic contamination
  In-line metrology for pre-gate, hydrophobic surface preparation such as % oxygen
- Extending existing particle identification methods to in-line product wafer capability
- In-line and in situ metrology of thin film thickness uniformity and composition for gate dielectric (requirement is for control of voltage threshold distributions) and other layers must be extended to 4 nm layers
- Off-line analytical technology also requires improved cycle time, sensitivity and resolution
- Off-line user facilities with unique capabilities allowing calibration of other methods

POTENTIAL SOLUTIONS

Near field optical microscopy (NFOM) systems capable of spectroscopic analyses have the potential of extending in-line defect identification and composition analysis to technology generations having 0.1 μm design rules and beyond. Therefore, NFOM should be given special attention for research and development efforts. Other techniques are listed in the solutions roadmap. User facilities that allow a broad-based access to unique capabilities include the synchrotron x-ray centers and heavy ion backscattering for trace analysis of surface metallic impurities, and accelerator mass spectrometry for analysis of metallic impurities in the region of polished, epi, and SOI wafers used in the fabrication of IC devices. Off-line analytical equipment is needed to improve analysis cycle time and meet the challenge imposed by decreasing device size by smaller spot ion guns and addressable sample stages.

STARTING MATERIALS

The time lines for the priority needs for starting materials metrology are listed in the detailed potential solutions (Figure 3). Again, development of large diameter wafer metrology tools is a critical need. Light scattering from surface defects such as microroughness limit applicability of existing optical particle/defect detection equipment to development and qualification of future starting materials, large wafers, silicon on insulator wafers, and epi wafers.

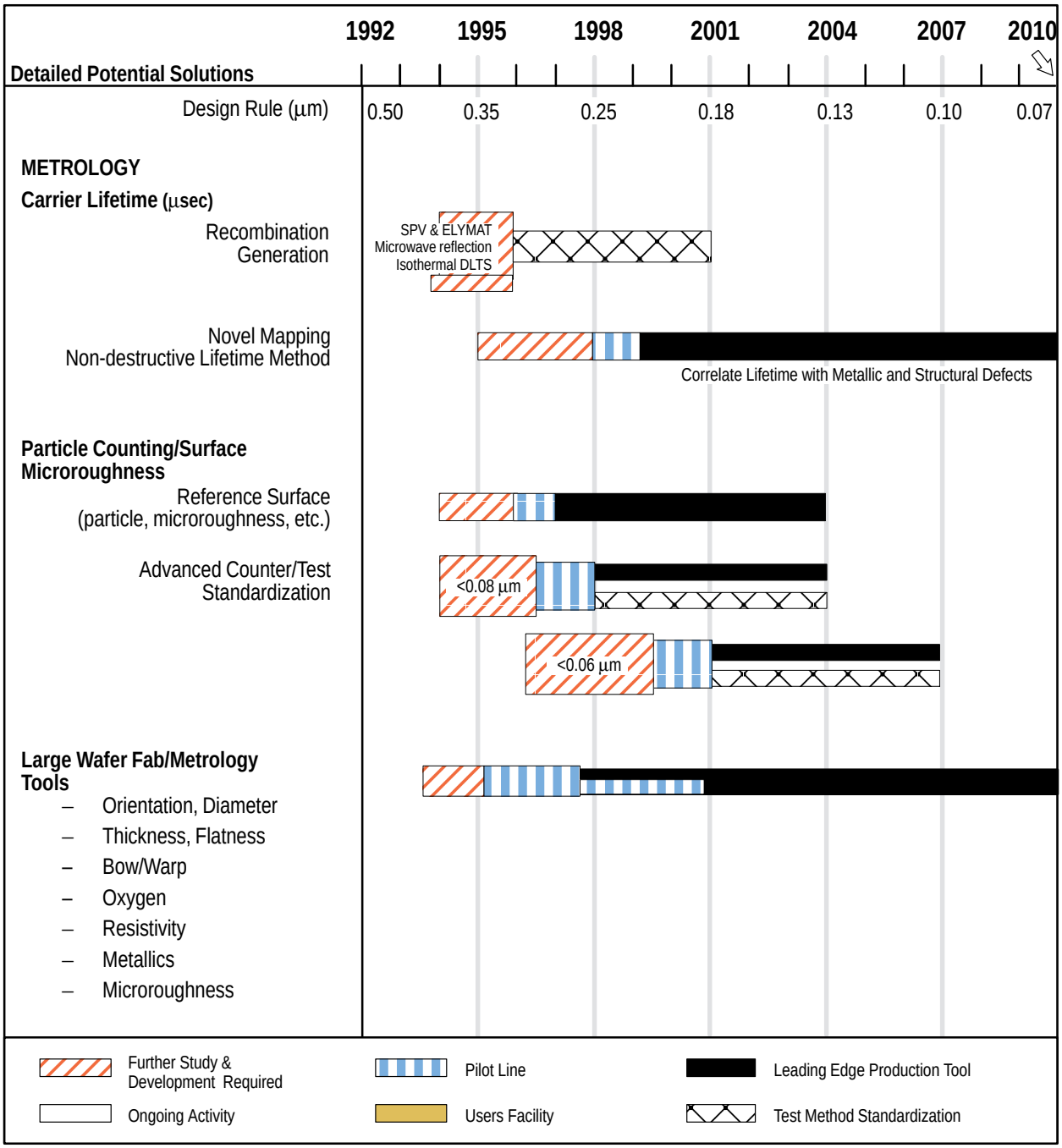


Figure 3 Starting Materials

Figure 3 Note:

There are three main categories of the Starting Materials metrology needs. The push for large diameter wafers will require some 300mm capable metrology tools as early as the fourth quarter of 1995. The highest priority tools are listed, and a more detailed 300mm metrology tool roadmap is under development. The new bare wafer particle detection tools and standardization of carrier lifetime measurements are driven by both the design rule requirements and the large diameter wafer needs.

THIN FILM METROLOGY NEEDS

Precise measurements of thin film parameters for future gate dielectrics less than ten atomic layers thick will be required for process control. Control of an area-averaged sample to less than one atomic layer will require improvements in tools, methods, and reference materials for precision and accuracy (Figure 4). Thickness uniformity for gate dielectrics is required for keeping tight distributions of threshold voltage.

Major issues involve:

- The understanding and modeling of the materials science of the films, interfaces, and their effect on film parameters
- The development of adequate tools and methodology by equipment manufacturers
- The push for in situ controls

PARTICLE COMPOSITION ANALYSIS

Characterization of the composition of particles on whole product wafers is presently done by manual inspection with optical microscopes and by x-ray fluorescence using energy dispersive spectroscopy (EDS) in scanning electron microscopes (SEM) equipped with automated whole wafer stages. In FAB, manual inspection must become automated, and the defect classification algorithms will require information from in-/off-line systems such as SEM/EDS (Figure 5a). The size limitations of SEM/EDS varies according to the composition of the particles and the background layer (Si substrate, oxide layer, aluminum metal lines, etc.). The limit of 0.5 μm particles/defects listed on the potential solutions roadmap is a rough guide. The process-based requirements by technology generation specify a need for analysis of 0.08 μm particles/defects. The consensus roadmap lists Auger, ToF-SIMS, and NFOM as potential near term technology for whole, product wafer particle/defect characterization (Figure 5b). New x-ray detector technology may allow high-energy resolution analysis of x-ray fluorescence excited by low energy electron beams.

*Limited by direct tunneling

Figure 4 Thin Film Metrology

Figure 4 Note:

Future IC technologies will use thinner gate dielectrics and epitaxial silicon layers. The NTRS data for gate dielectric and epi thickness and uniformity are listed along with the metrology tools that the Materials and Bulk Processes Metrology Roadmap participants selected for these applications. Total Wafer Thickness refers to a new optical measurement method for total wafer thickness. Low Z X-ray Fluorescence is also known as low energy x-ray fluorescence. Since FAB compatible FT–IR systems already measure epi layer thickness, continuous software and hardware improvements are expected to extend this capability.

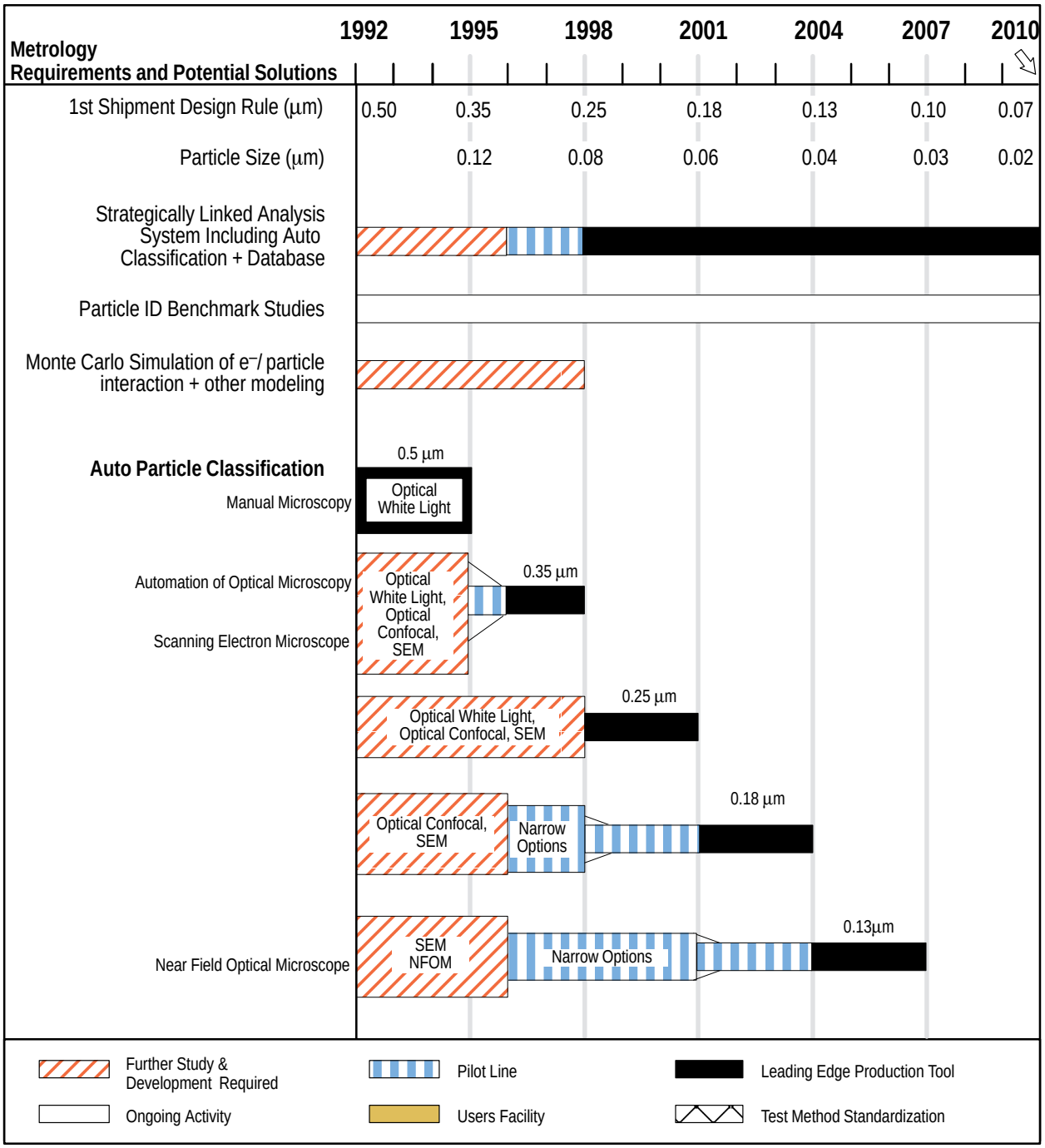
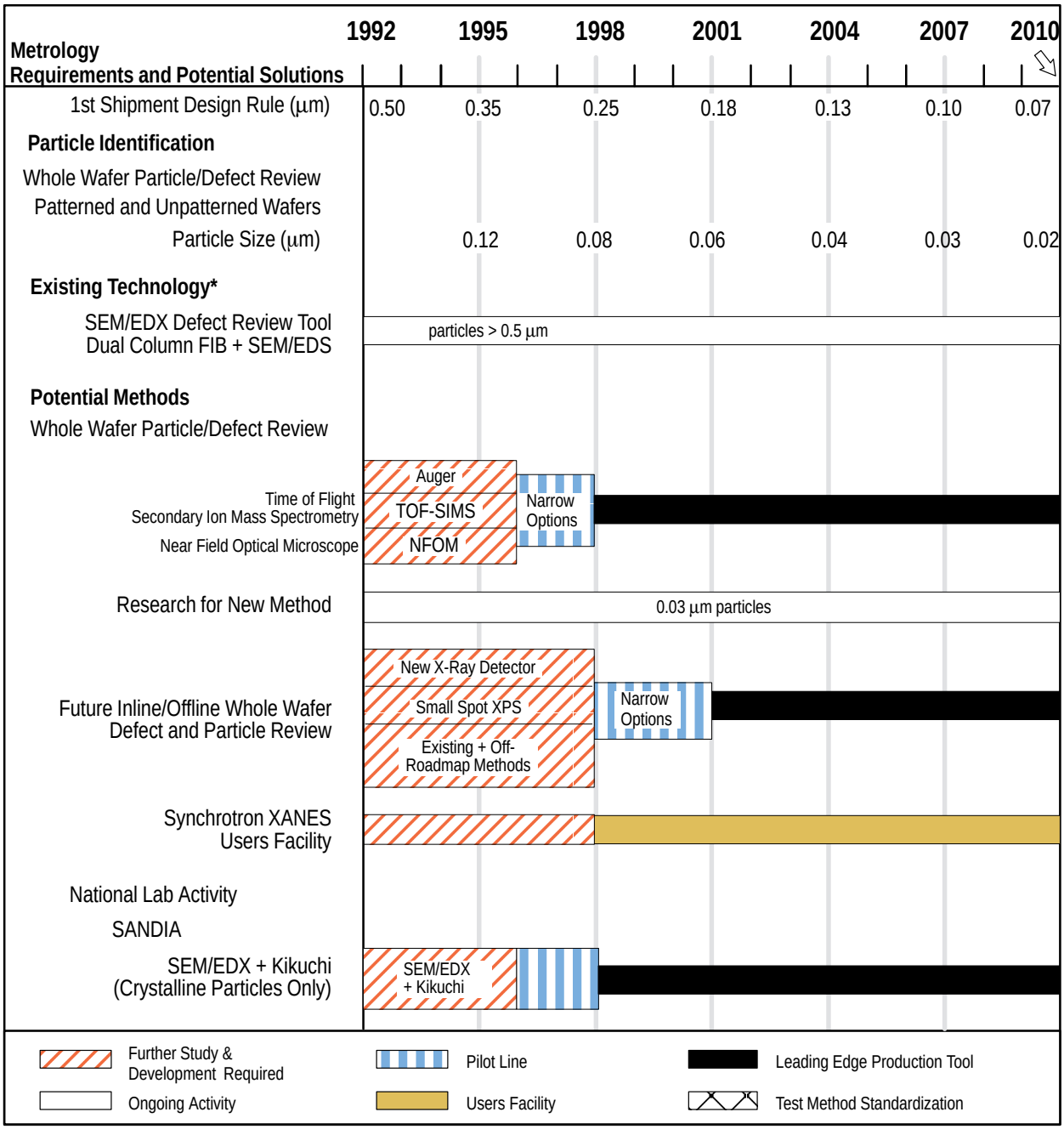


Figure 5a Particle Composition Analysis

Figure 5a Note:

In this figure, the NTRS specifications for minimum particle size are listed along with the requirement for networked analytical systems, benchmark studies, and modelling of electron beam and ion beam – particle interactions. Off-Line particle composition analysis is a part of particle sourcing that begins in the FAB when manual, optical microscopy is used to characterize particles and defects. The Auto Particle Classification information describes the effort to replace manual microscopy with in-line automated particle sourcing tools. The requirements for defect detection are listed in the Contamination Free Manufacturing section of the Materials and Bulk Processes Roadmap in the NTRS. Data management systems are a key part of rapid yield learning using this type of technology.



*Estimated limit for pattern wafer particle analysis using existing EDS detectors. Some samples may allow analysis of smaller particles. Combined SEM / EDS / Auger systems may be developed for sub 0.5 µm particles.

Figure 5b Particle Composition Analysis

Figure 5b Note:

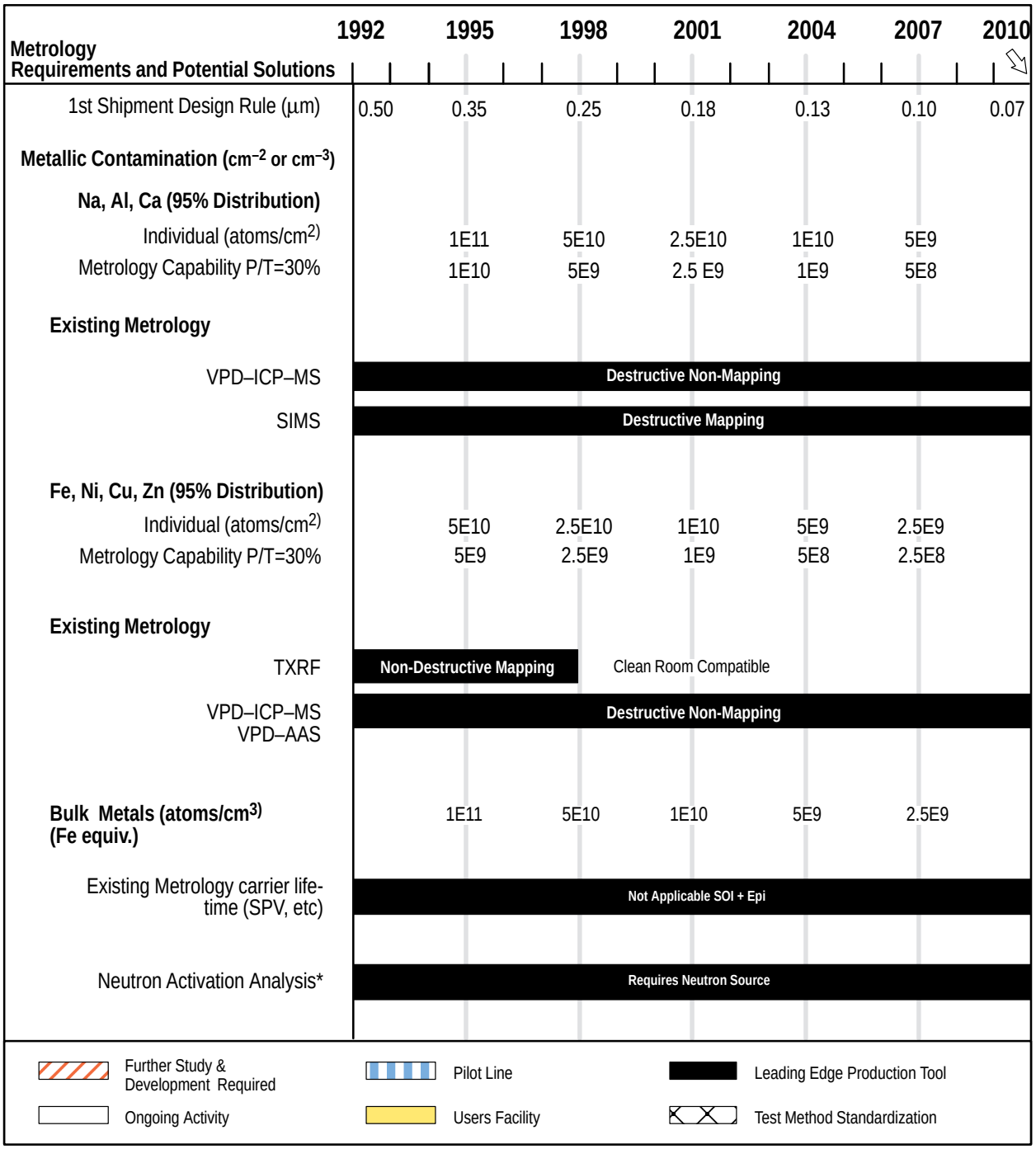
Particle identification using whole wafer defect review tools is described in figure 5b. Existing SEM/EDS systems and dual column SEM/EDS– FIB systems will continue to play a key role in particle and defect analysis. Although high electron beam voltage SEM/EDS particle/defect characterization is inadequate for sub 0.5 µm particle analysis on future product wafers, whole wafer defect review systems will continue to be used and developed. For example, SEM/EDS may be combined with other methods such as Auger Spectroscopy. The potential methods for analysis of particle and defect sizes listed in the NTRS is divided into near term solutions (Auger [UHV and in SEM/EDX], ToF-SIMS, and NFOM), methods presently undergoing basic development (e.g., the microcalorimeter x-ray detector), and novel methods such as synchrotron XANES and Kikuchi pattern analysis. The microcalorimeter x-ray detector is being developed for high energy resolution detection of low and high energy x-rays. SEM/microcalorimeter analysis capabilities should be evaluated. Contamination control engineers have indicated that most particles are not crystalline, and this was thought to limit the usefulness of the Kikuchi analysis for this application. Possible new methods include a practical post-ionization (of sputtered neutrals) upgrade to TOF–SIMS.

METALLIC AND ORGANIC CONTAMINATION ANALYSIS

The process driven requirements of decreasing levels of surface contaminants increases present and future gaps in metals analysis capabilities. The nature of metallic contamination from implanters may often differ from less energetic sources. Special attention to ultra-clean sample handling and preparation will be required especially for alkali metal analysis. Many 200 mm wafer metrology tools are not available. Three areas require special attention for both starting materials and surface preparation (Figures 6a and b). The lack of standard methods and reference materials for analysis of metallic and organic contamination and carrier lifetime is an impediment to effective commerce in starting materials and process development for surface preparation and starting materials. Several analysis methods are routinely used, and consensus standards for cross-calibrating methods are in development. Non-destructive mapping of light element and transition metal (at detection limits required by future specifications) contamination has been specified as a major requirement (Figure 6b). The use of Vapor Phase Decomposition sampling followed by High Mass Resolution ICP-MS provides destructive characterization of alkali and transition metals at levels lower than 1x109 at/cm2 (200 mm and 300 mm) (Figure 6a). Great care should be used when VPD-TXRF is used because of uneven metal concentrations at the VPD spot resulting form droplet evaporation. VPD on 300 mm wafers is difficult due to evaporation of the collecting droplet during sampling. Special mention should be given to the need for users' facilities having analysis equipment with unique capabilities for ultra-trace characterization (Figure 6b). These include the use of synchrotron x-ray centers for particle and surface metallic impurities, heavy ion backscattering spectrometry (HIBS) for trace analysis of surface metallic impurities, and the use of accelerator mass spectrometry for analysis of metallic impurities in the region of SOI wafers used in the fabrication of IC devices. HIBS provides a convenient method for calibration of reference materials. Synchrotron TXRF has the capability of selecting radiation that allows analysis of light-element contamination on silicon surfaces. Off-line analytical technology also requires attention. TOF-SIMS may provide destructive mapping of surface contamination. Smaller spot ion guns and addressable sample stages for surface analysis equipment are two examples.

IMPLANT CALIBRATION AND 1-D DOPANT PROFILING

In-line, non-destructive implant process control methods are challenged by existing manufacturing needs. Consensus requirements indicate that repeatability should be given priority over accuracy. Implant reference materials are primarily needed for process transfer and for industry reference. Four point probe resistivity measurement will continue to provide critical characterization. Methods that monitor the amount of implant-induced lattice damage provide non-destructive characterization and low-dose sensitivity, and monitor stability and sensitivity are critical needs in this regime. Junction depth control is typically monitored off-line by SIMS and SRP (Figure 7). Existing SIMS tools that utilize low energy probe ion beam have demonstrated very shallow junction measurement that meets roadmap requirements beyond 0.25 μm design rules. SRP technology that meets future requirements has been demonstrated, but is not yet typical.



*At least two SEMATECH member companies have routinely utilized neutron activation analysis for silicon materials qualification.

Figure 6a Metallic and Organic Contamination Analysis

Figure 6a Note:

In figure 6a, NTRS (as listed in both the Starting Materials and Surface Preparation sections of the MBP Roadmap) requirements for light element, transition metals and Na, and bulk Fe contamination along with existing metrology methods used by IC manufacturers. SIMS analysis of transition metal impurities was not listed in the existing metrology section since it was considered to be under development. Since the requirement is for non-destructive, product wafer analysis at the NTRS detection limit levels, existing methods will not meet roadmap needs.

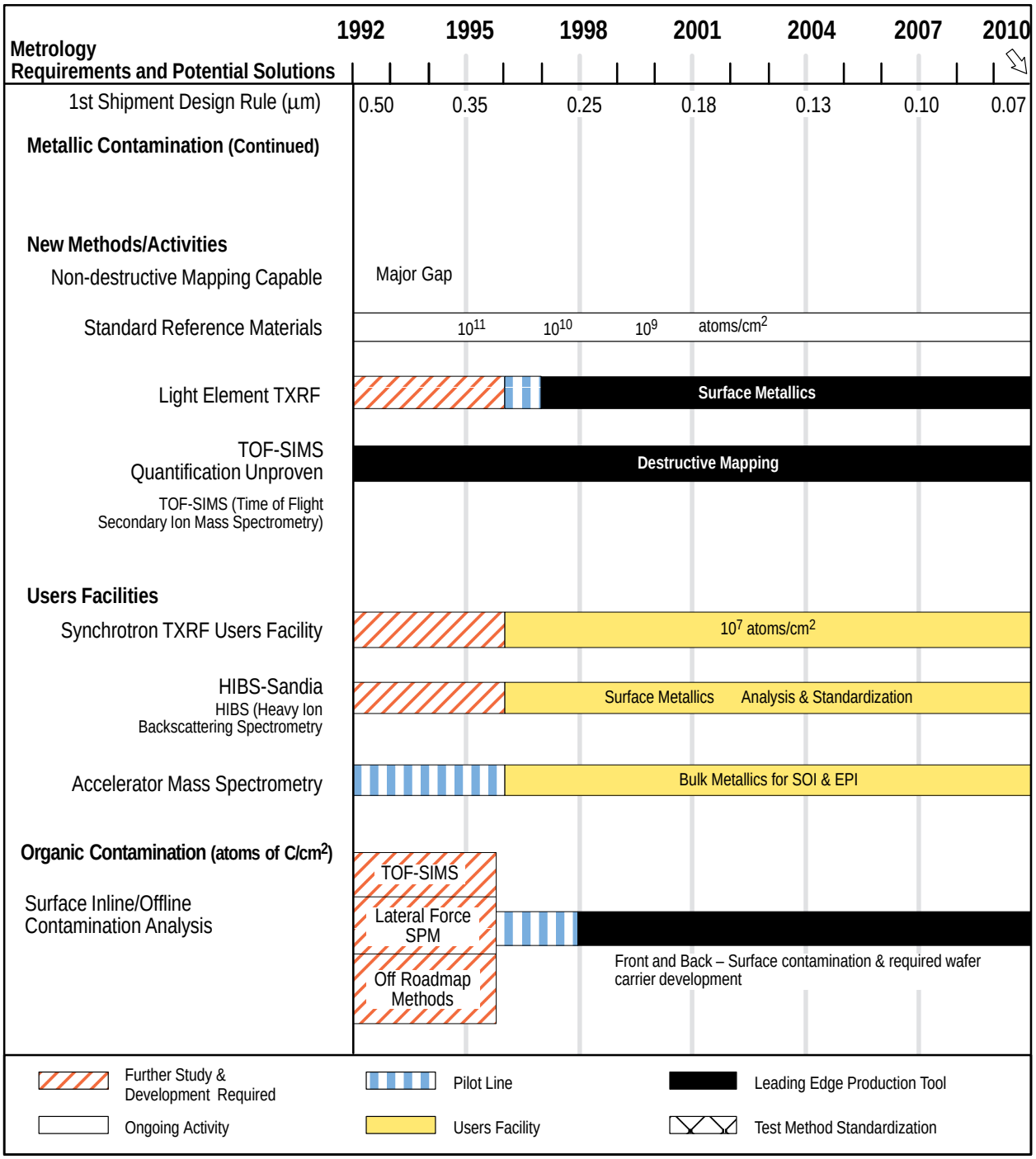


Figure 6b Metallic and Organic Contamination Analysis

Figure 6b Note:

The potential solutions for metallic and organic contamination analysis are listed. User facilities may be used to provide unique (eg., Heavy Ion Backscattering Spectrometry and Accelerator Mass Spectrometry) or high cost (eg., synchrotron TXRF). Pilot line tools would refer to initial or beta site tools when the systems are used off–line. TXRF systems capable of light element analysis were considered a high priority. Improvements in TXRF sensitivity are also expected. Some SEMATECH member company analytical laboratory representatives have indicated that large diameter wafers might be returned for further processing after SIMS analysis if the wafer environment was suitable. Therefore, it was included in the potential solutions section.

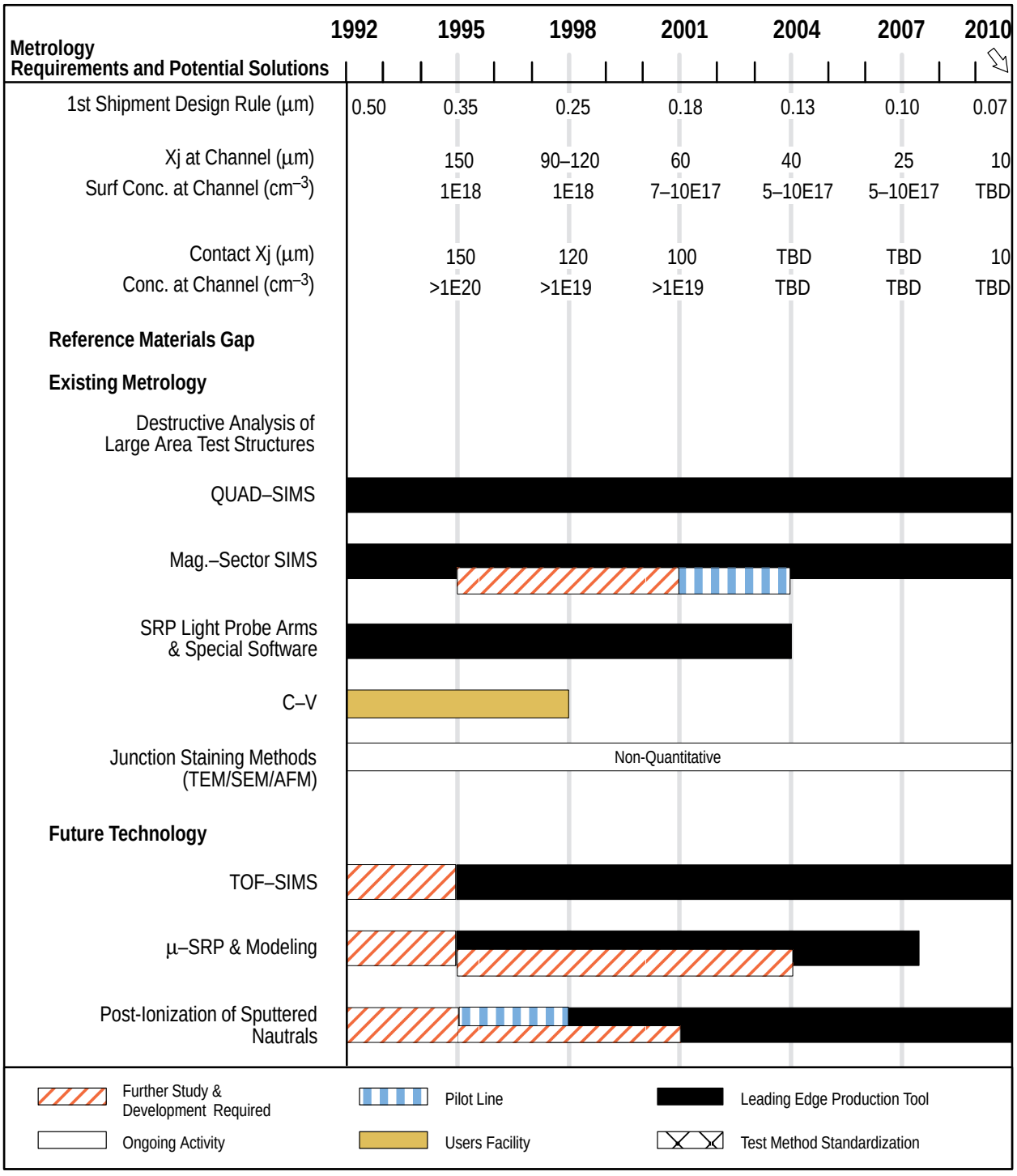


Figure 7 Doping 1-D Characterization

Figure 7 Note:

Junction depths and dopant concentration levels are listed for transistor channel and contact regions. Existing metrology methods provide destructive analysis of large structures. There is no fundamental reason that magnetic sector SIMS, Quad SIMS and ToF-SIMS could not all meet ultra shallow junction analysis requirements. SRP is continuously being developed, and it is expected that micro-SRP will be used for 1-D and 2-D dopant profiling. Post-ionization of sputtered neutrals refers to both the resonant and non-resonant laser ionization of neutral atoms sputtered by an ion beam system (typically a SIMS).

LITHOGRAPHY

Wafer-level metrology will continue to be driven by the critical dimension (CD) and overlay requirements of advanced lithographic processes. Currently output metrology based on scanning electron microscope images for CD and brightfield optical overlay measurement using SEMI Standard "box-in-box" targets are used almost exclusively for 0.5 μm process control and are expected to dominate through 0.25 μm design rules. Current CD and registration metrology systems for mask manufacturing are capable for process control through 0.35 μm design rules and can be extended to 0.25 μm.

CURRENT TECHNOLOGY STATUS

Brightfield optical metrology is the technique of choice for 0.5 μm, with modifications such as darkfield and phase contrast imaging being used to carry optical overlay metrology through the 0.13 μm design generation. Process integration issues may preclude the use of features large enough to be reliably detected using optical imaging and thus may limit the extension of this technique beyond 0.13 μm.

CD SEM measurement capability is marginally capable at 0.5 μm design rules. At 0.35 μm and below, the use of high throughput CD SEMs is expected to bridge the gap between marginal measurement capability and advanced process control requirements by improving estimates of process characteristics through averaging and measurement of actual circuit features.

In mask manufacturing, output metrology is expected to be the primary mode of operation through the 250/180 nm generation. Continued emphasis on output metrology for process control and the development of standards for CD measurement and calibration of registration tools are required (Figure 8). A summary version of Figure 8 can be found in the Lithography section of the NTRS.

Table 1 Critical Level Wafer Metrology Requirements
(from the Lithography section of the National Technology Roadmap for Semiconductors)

	1995 0.35 μm	*1998 0.25 μm*	*2001 0.18 μm*	*2004 0.13 μm*	*2007 0.10 μm*	*2010 0.07 μm*
Gate CD Tolerance (nm)	35	25	18	13	10	7
Final CD output metrology (nm) 3σ reproducibility [atoms]	3.5 [8]	2.5 [6]	1.8 [4]	Transition to inline and in situ control required.		
Overlay (OL) tolerance (nm)	100	75	50	40	30	20
OL output metrology 3σ reproducibility (nm)	10	7.5	5	4	3	2
OL Process Control Metrology: Pre-expose alignment mark distortion estimate (nm)	10	7.5	5	4	3	Sensor/ method required

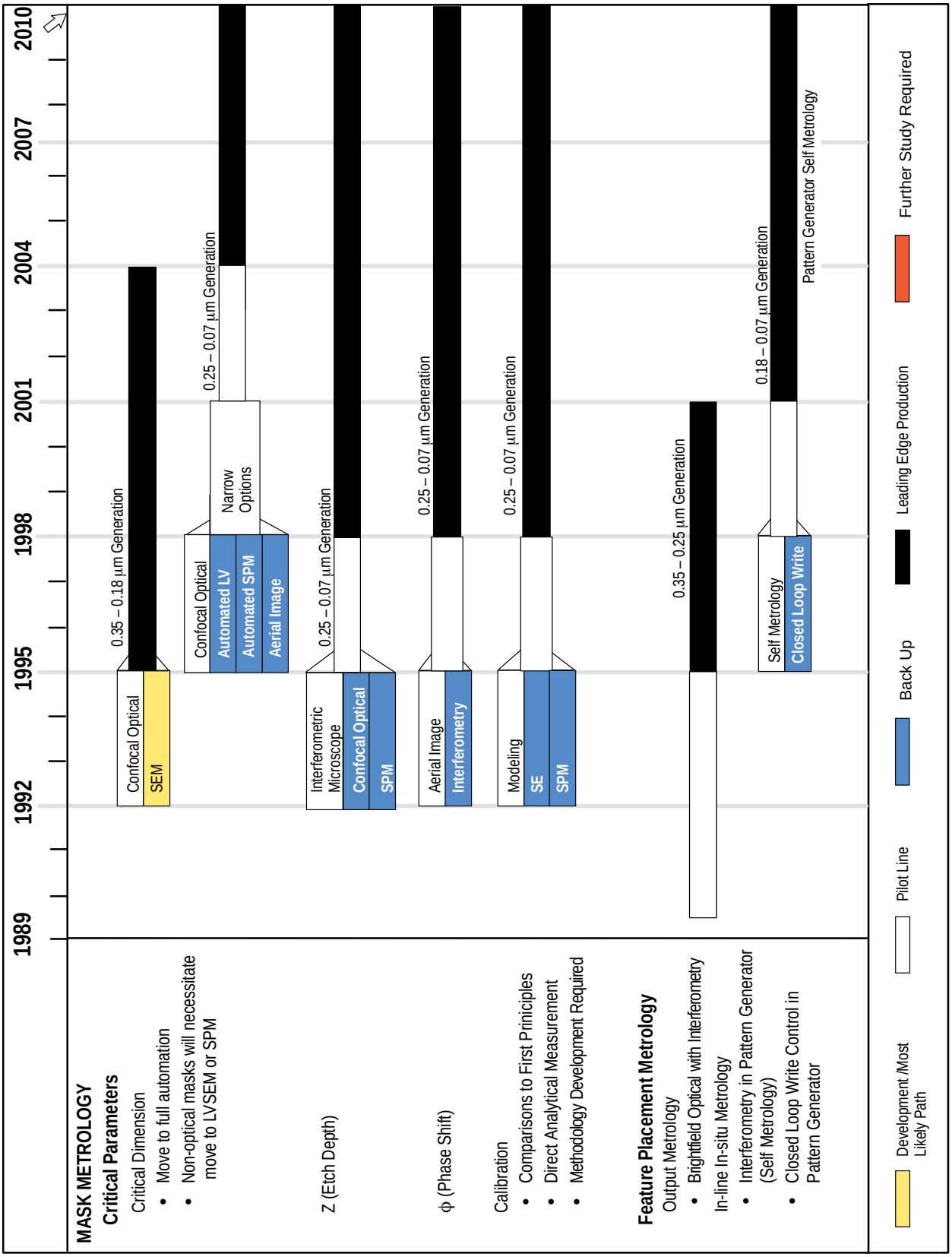


Figure 8 Critical Level Mask Metrology Roadmap

COMMENTS AND PRIORITIES

Successful overlay control will hinge on the industry's ability to develop targets that exhibit reduced sensitivity to processing. Key process issues to be addressed are target asymmetries associated with resist coat over topography, radial asymmetry of metal and dielectric films deposited on the wafer, and the design of measurement structures that are more robust to chemical mechanical polish (CMP).

The requirements for Wafer Level CD Metrology were listed in the NTRS and are presented in Table 1 for completeness. At 0.25 μm design rules it will be necessary to begin driving CD control through the use of in situ metrology. The evaluation to in situ metrology is driven by productivity and yield improvement requirements. Process improvements in CD process control will also require the use of new forms of metrology as SEM and other techniques approach atomic dimensions (Figure 9). These control methods will require the development of new sensor technologies to monitor resist coat thickness and uniformity, photo-active compound (PAC)/photo-acid generator (PAG) and solvent concentration, pre/post bake temperature uniformity, and develop uniformity. The driver behind this proliferation of sensors is the realization that complex interactions between the incoming wafer, coat, bake, expose, and develop frequently can not be corrected by subsequent processing without adversely affecting device performance characteristics. As an added benefit, 100% sampling of wafers using in situ metrology will stay the trend toward ever increasing numbers of measurements following the develop step and reduce output metrology to a short duration, small sample, quality control function (Figure 9).

There is strong pull from industry to develop a more consistent and reproducible method of measuring CD and overlay (Figure 9). This pull stems from a desire to reduce the amount of characterization time required to qualify measurement results and a critical need to precisely determine the magnitude of process-induced biases in CDs and pattern alignment. Success in this area will require the development of measurement techniques that are independent of level and context. Specific examples include the elimination of variable calibration offsets for dense relative to isolated line CDs and level specific TIS corrections for overlay.

The integrity of measurements for both CD and overlay must be improved through the development of more robust and accurate measurement techniques or through the use of redundancy and error checking to identify when incorrect measurements are made.

Streamlining the flow of large amounts of data from highly automated CD and overlay instrumentation is another major impediment to easy and efficient implementation of measurement and control systems. Standardization on a GEM messaging set for use with CD and overlay equipment is required to relieve the problem.

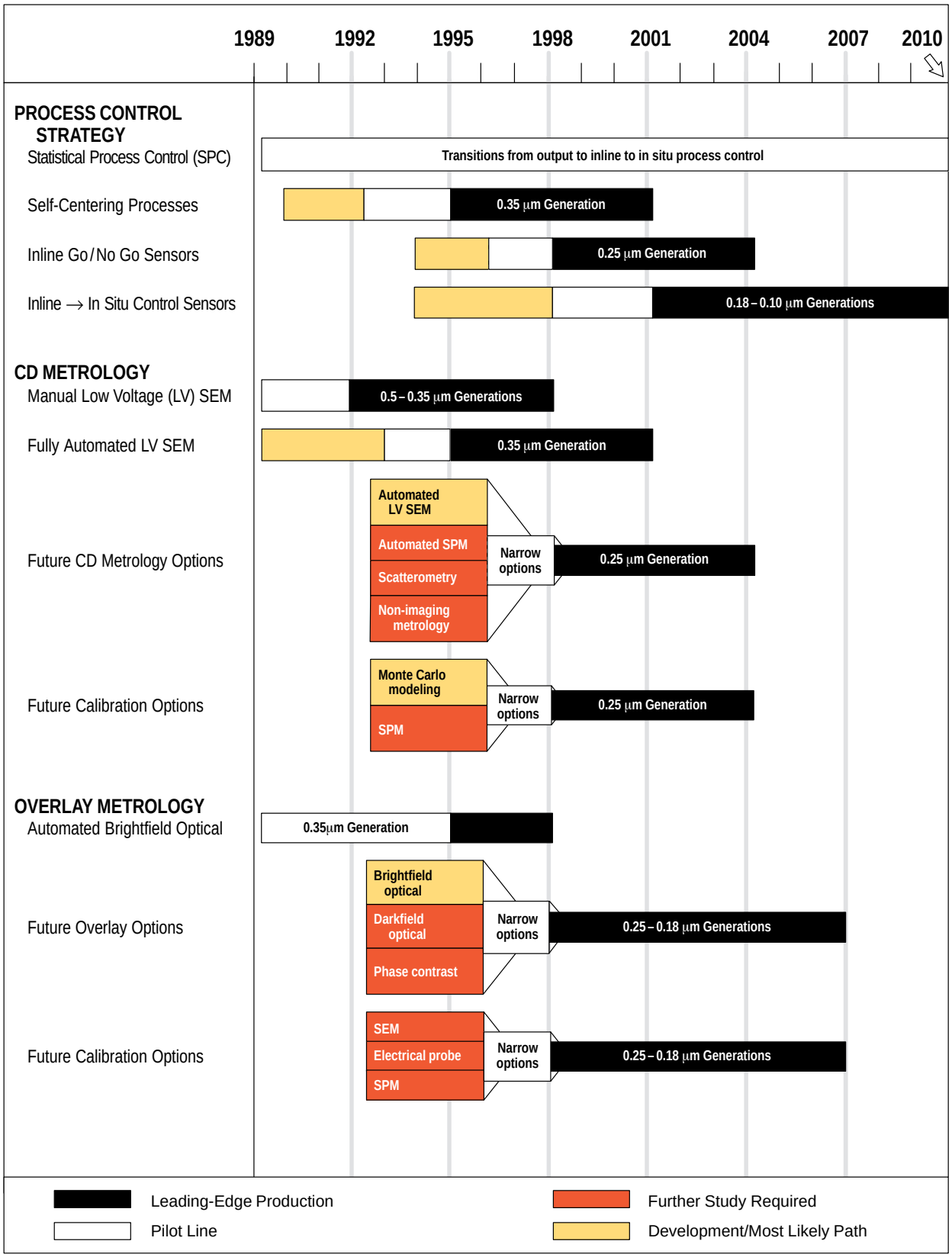


Figure 9 Critical Level Wafer Metrology Potential Solutions Roadmap

INTERCONNECTS

The interconnects section covers the dielectric, metal film formation, and etch processes that are sometimes referred to as the back end of the line fabrication steps. Development activities include planarization processes such as chemical-mechanical polishing and advanced materials systems such as copper interconnects and low dielectric constant polymers. The biggest issue for etch and deposition technologies is fabrication of high aspect ratio features for 0.18 μm design rule ICs. Areas of overlapping metrology activity include particle detection and identification, surface metallic and organic contamination analysis, and critical dimension measurement.

CURRENT TECHNOLOGY STATUS

Process development is done using electrical test structures, and process control is mostly off- and in-line. New interconnect tools and processes are evaluated for stress migration and electromigration, plasma etch damage of gate oxides, and failure inducing particles/defects. Work is underway to standardize electrical test structures that allows collection of data for development of predictive interconnect failure models. SEMATECH's SPIDER test structure has become an accepted standard method for evaluation of gate oxide damage.

Some member companies report that in-line etch damage process control can be done using surface charge imaging. Use of this capability requires SPC of the metrology tool itself and knowledge of historical charge maps.

COMMENTS AND PRIORITIES

The priority needs for Interconnect technology is summarized in the Crosscut Technology section of the Interconnects roadmap. These are listed by the priority listed in the NTRS.

1. CD, profile, and/or edge roughness for polysilicon, high aspect ratio (dielectric) vias, and metal lines
2. Film thickness on patterned wafers of barrier layers (eg., TiN), conductive films such as TiSi2 contacts, new inter-metal dielectrics
3. Ex situ and in situ evaluation of cleanliness of high aspect ratio contact/via
4. Sensors for in situ process control
5. Surface planarity (flatness and topology) within lithographic field to ensure depth of focus at lithography
6. Post-etch residue control to prevent corrosive precursors left on metal surfaces and contamination-induced delamination
7. Film morphology

NEEDS

Measurement of properties of product wafers must be developed, and process and tool models should be used to guide application of in situ sensors (Figure 10). These needs include critical feature size, film thickness, contamination, surface planarity, and critical process conditions. Metrology will find its widest use as a means of rapid yield learning, and only selected measurements will be used in routine manufacture. Existing modeling of particle formation and deposition inside a plasma has the potential of guiding both chamber design and particle sensor deployment. End point control for chemical mechanical polishing is a short term, high priority issue. The detailed solutions chart shows known metrology activity. The in situ light scattering approach to CD measurement may find its initial use in the development of Interconnect tools and processes (Figure 10).

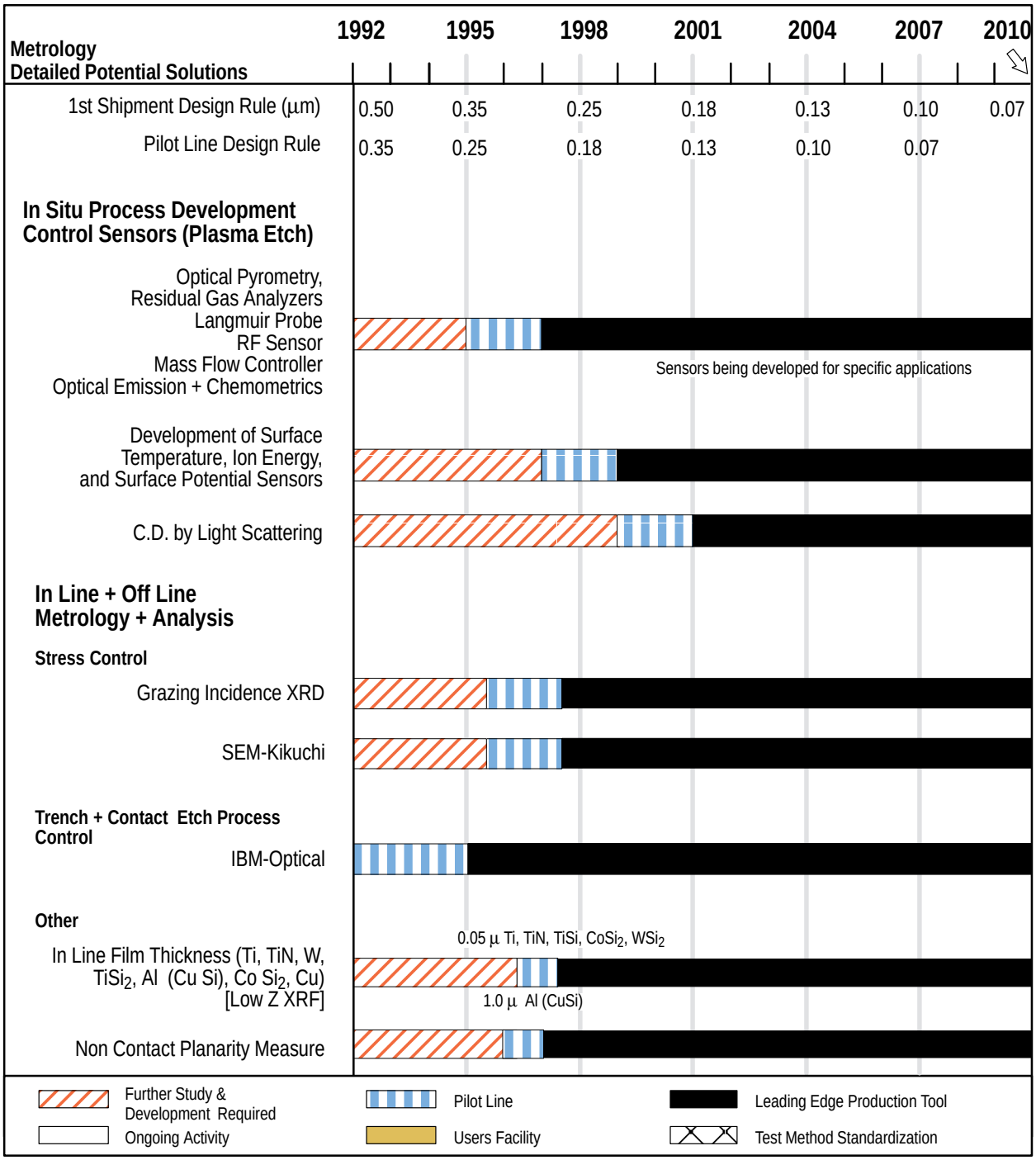


Figure 10 Interconnects

Figure 10 Note:

The potential solutions for Interconnect metrology are predicted to emphasize in-situ sensors for plasma process control. The roadmap for these sensors is based on the Plasma Diagnostics Workshop of Sept. 16, 1993. These sensors may be used during process development and a decrease in sensor use is expected for manufacturing, and the pilot line symbol refers to sensors on pilot line process tools. Process state sensors for plasma etch processes include monitoring the plasma and the ambient gas in the chamber. Wafer state sensors have a longer development period. Wafer state sensors will be used to control damage due to ion impact during etch processes. Etch uniformity and endpoint control are two focuses of the scatterometry measurement of critical dimensions. In-line and off-line methods for stress, trench, and contact etch process control are listed. Rapid characterization of contact and via openings for sub 0.25µm technologies may be done using novel optical methods. Low Z XRF has been suggested as an in-line method for monitoring the uniformity of thin barrier and contact layers. No method is specified for non-contact planarity measurement.

FACTORY INTEGRATION

The Factory Integration section discusses the implementation of all other process and design sections into a cost-effective factory. This section covers the manufacturing processes of the wafer fab, assembly, packaging, and test. Of key importance to metrology development are the "fab level" discussions of process control, material handling, environmental control (especially wafer environment), and information systems for the entire fab. The data management and process control issues are examples of information systems needs that will evolve to the "fab level." These systems are a key to use of metrology for rapid yield learning. Factory integration systems must comprehend off-line analysis needs.

COMMENTS AND PRIORITIES

The metrology needs can be found in the section on wafer environment control, and facilities technology. Minienvironments systems must be certified for cleanliness levels, and organic contamination is a well documented concern. Fluid delivery systems may utilize sensors to monitor excursions in contamination levels resulting from fluid transport. A fluid purity requirements roadmap is being developed during 1994, and it should provide point-of-use fluid purity requirements by technology generation.

MEASUREMENT CAPABILITY ANALYSIS

Before introducing a metrology tool into a pilot line or new fab, the tool must be tested for its measurement capability. The selection of a fab metrology tool is based on cost of ownership (tool cost, uptime, fab space, etc.) and measurement capability. Introduction of a new method that utilizes an existing tool also requires a measurement capability analysis. Process control is not possible unless metrology meets the required measurement capability, and SEMATECH typically expects a precision-to-tolerence ratio of < 30%. The SEMATECH measurement capability analysis has become widely accepted by SEMATECH member companies and process tool suppliers. It is critical that future metrology technology include measurement capability analysis as a part of each stage of its development.

Although some off-line measurements are not used to control processes, they are required to have known precision. The measurement standard deviation (including error from multiple operators) used below should be known for each off-line tool.

Statistical Process Control (SPC) is used to maintain a stable process. In concert with statistical experimental design, capable processes are achieved (ie., process performance consistently falls within the tolerance limits that are required for high-yield manufacture). In order to accomplish this, the metrology tool must meet a criterion for the precision-to-tolerance ratio (P/T = 6 standard deviations of the measurement distribution/process tolerance). The process tolerance is the upper specification limit for the measured parameter-lower limit. The measurement standard deviation includes the (long-term error caused by equipment stability and multiple operators) reproducibility and (short-term error) repeatability of the measurement. The square of measurement standard deviation is the sum of the squares of the reproducibility and the repeatability. **One clear message from measurement capability analysis is that it is more important for a method to have a small measurement**

standard deviation than is accuracy. It is relatively easy to correct errors in accuracy (or bias). SEMATECH Technology Transfer #91090709A-ENG was used in the preparation of this section.

Note: P/T should not be confused with the process capability, C_p, which is defined as (upper specification limit for the measured parameter – lower limit)/estimated process standard deviation. The process standard deviation includes the product distribution contribution and the measurement error.

LIST OF ABBREVIATIONS

2-D	Two Dimensional
AAS	Atomic Adsorption Spectroscopy
AFM	Atomic Force Microscopy
APIMS	Atmospheric Pressure Ionization Mass Spectroscopy
e	symbol for an electron
EDS	Energy Dispersive Spectroscopy
EPI	Epitaxial Silicon Wafers
FIB	Focus Ion Beam System
FTIR	Fourier Transform Infra Red Spectroscopy
HIBS	Heavy Ion Backscattering Spectrometry
ICP-MS	Inductively Coupled Plasma Mass Spectrometry
NFOM	Near Field Optical Microscopy
RBS	Rutherford Backscattering Spectrometry
SE	Spectroscopic Ellipsometry
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
SNOM	Scanning Near Field Optical Microscopy
SPM	Scanning Probe Microscopy
SPV	Surface Photo Voltage
SRP	Spreading Resistance Probe
STM	Scanning Tunneling Microscopy
STM-spectroscopy	I-V curves obtained using STM
C-V M or SCM	Scanning Capacitance Microscopy
TEM	Transmission Electron Microscopy
ToF-SIMS	Time of Flight SIMS
TXRF or TRXRF	Total Reflection X-ray Fluorescence
VASE	Variable Angle Spectroscopic Ellipsometry
VPD	Vapor Phase Decomposition
XANES	X-ray Adsorption Near Edge Structure Spectroscopy
XPS	X-ray Photoelectron Spectroscopy
XRF	X-ray Fluorescence

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