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Merced Slips to Mid-2000

Delay Jeopardizes Attempt to Gain Performance Lead

by Linley Gwennap

Note: This is a summary of the full article, which is available only to Microprocessor Report subscribers.

Reality has reached out and tossed sand into the gears of Intel's product-development machinery. The company regretfully reported that an eight-month schedule slip has pushed the first volume shipments of its Merced processor from late 1999 to mid-2000. This slip will delay IA-64's penetration of the workstation and server markets and make it more difficult for Merced to achieve the performance lead, as Figure 1 shows.

Delay Caused by Poor Planning

Designing a new processor and a new instruction-set architecture (ISA) from scratch is always a long and daunting task. By pushing into the next decade, however, Intel's IA-64 effort is breaking two previous public commitments and is threatening to set a new record for gestation period.

The IA-64 effort was formally started in early 1994, when Intel and HP first began working together. Last fall, the company was confident enough in its progress to disclose the first details of the IA-64 instruction set (see MPR 10/27/97, p. 1) and reconfirm its commitment to 1999 shipments. At Microprocessor Forum, Intel's Fred Pollack promised that Merced would deliver "industry-leading performance" when it shipped. The design team at this point consisted of several hundred engineers, and the logical design was nearing completion.

Despite (or perhaps because of) this enormous staffing level, keeping the Merced program on schedule continued to be difficult. After a recent schedule review, senior management was shocked to discover that the chip was nowhere near tape out and in fact could not be expected to ship until the middle of 2000. Since Intel had publicly committed to 1999 shipments, it was forced to publicly acknowledge the change in plans.

Competitive Performance May Suffer

Intel denies rumors that Merced is having trouble meeting its clock-speed and performance goals. Even if its performance is still on target, however, Merced will have more of a problem exceeding the competition than it would have had in 1999. Based on Moore's Law (a concept Intel should be familiar with), competitive performance should increase by about 25% during a six-month slip.

Part of Merced's performance comes from its use of 0.18-micron process technology, giving it an advantage over 0.25-micron processors. Under the previous plan, Merced was to be one of the first products off Intel's—or anyone else's—0.18-micron process. By mid-2000, however, 0.18-micron technology will be in common use for leading-edge microprocessors.

In particular, Intel is committed to delivering a 0.18-micron version of the 21264 processor to Digital as part of the two companies' foundry agreement (see MPR 11/17/97, p. 1). We expect that chip to reach 65 SPECint95 and 100 SPECfp95. Similarly, Sun's UltraSparc-3 (see MPR 10/27/97, p. 29) should also ship in a 0.18-micron process by that time, achieving 45 SPECint95 and 80 SPECfp95.

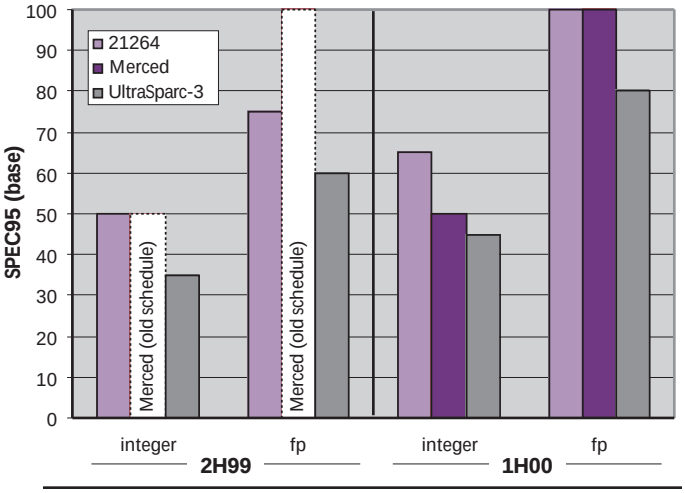

Figure 1. Merced had a good shot at gaining the performance lead in 2H99 on both integer and floating-point benchmarks, but by mid-2000 it could be merely among the pack in performance, particularly on the integer side. (Source: MDR estimates)

Since the schedule slip does little to improve Merced's performance, we expect it will have a tough time exceeding the integer performance of the 0.18-micron 21264. And its performance advantage over processors such as UltraSparc-3 and IBM's Power3 will be narrowed. Thus, Intel may not be able to claim bragging rights for its new architecture.

Sources indicate that Intel and HP are now pinning their performance hopes on the second-generation IA-64 processor, code-named McKinley. Intel had previously committed to delivering this device in 2001 with twice the performance of Merced in the same CMOS process. The company says the Merced slip will not affect McKinley, which is being developed by a separate design team. MI