Design of a Switched Opamp-based Bandpass Filter in a 0.35 μm CMOS Technology

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ABSTRACT

A fully differential bandpass filter based on the switched-opamp approach is designed in this work. It was realized in a 0.35 μm CMOS technology, and is able to operate from a single 1V supply voltage with a powerdrain of 230μW. As a main internal filter component, a fully differential switched opamp was also designed. Its common mode feedback circuit was implemented by using a switched capacitor network along with an error amplifier. Both the opamp and the filter were simulated with the Spectre program. Simulation results obtained by using the extracted circuit from the layout are presented.

1. INTRODUCTION

Both the battery-operated systems and the new submicron technologies require the use of a decreased power supply voltage and, then, the demand for circuits operating at very low power supply voltages (i.e., between 1 and 2V) is very high.

The switched capacitor (SC) technique has been proved to be an excellent analogue technique which shows superior features in various applications. Furthermore, for low cost integration, standard CMOS processes have to be used and SC circuits are well-suited for this technology. In particular, SC solutions for filters allow the realization of high accuracy with a low distortion and programmability on the time constants implemented, without demanding any tuning system as for continuous time filters. However, at very low power supply voltage its performance reduces drastically due to the reduction of the signal swing caused by switches. Thus, specific approaches, different from the standard SC design, have to be used to overcome this problem. Among the different strategies that have been proposed [1], [2], the switched opamp approach [3] is probably the more advantageous. In this technique, critical switches are eliminated and replaced by opamps which are switched on and off. Baschirotto and Castello [4] further developed the technique by making the circuit fully differential and separating the input and output common mode levels.

The aim of this paper is the design in a 0.35 μm CMOS technology of a bandpass filter based on the switched-opamp approach for Radio Data System (RDS) subcarrier detection. The filter operates at 1V and is clocked at f_s = 1 MHz. Its basic characteristics are the following: central frequency, f_0 = 58 kHz; quality factor, Q = 15; and, finally, voltage gain, A_V = 8. As an internal component of this filter, an appropiate switched opamp was also designed. Both the switched opamp and the bandpass filter were simulated with the Spectre program. All simulations were carried out by using the extracted circuit from the layout.

2. SWITCHED OPAMP DESIGN

2.1. Design of the opamp building blocks

The opamp was designed with a rail-to-rail output voltage range, and with a fully differential structure. In consequence, our switched opamp was based on two main funcional blocks: the core and the common-mode feedback (CMFB) circuit.

2.1.1. Core building block

The core design used in this work was proposed by Waltari and Halonen [5] that consists of a two stage amplifier (Figure 1). The input stage is based on a folded cascode topology, and a simple inverter provides the output stage of the amplifier. In order to obtain a fast opamp turn-on only the output stage is switched off acting on m16 (and m17), and during the inactive phase, the output terminals are connected to V_{DD}. The minimum power supply voltage is dictated by the m_4, m_6, m_8 device stack, giving:

$$V_{DD} - V_{SS} = V_{thP} + 3V_{DSsat}$$

Thus, the opamp is able to operate at just 1V in a 0.35 μm CMOS technology (V_{THp} = -650 mV).

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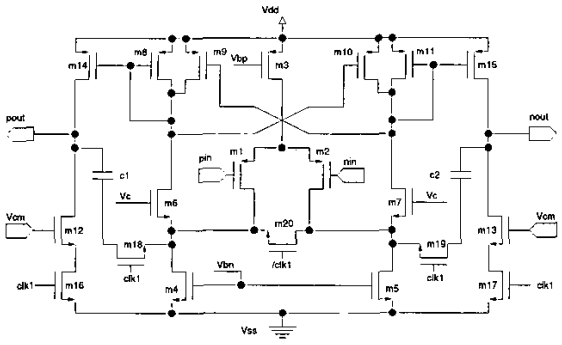

Fig. 1: Fully differential switched opamp core. Devices sizes are given in Table 1.

2.1.2. CMFB building block

In order to get a higher performance over a wide temperature and power supply ranges, an active SC solution for the CMFB circuit has been chosen (Figure 2), instead of the simple passive circuit suggested by Waltari and Halonen [5].

Our circuit includes an averaging capacitive network (C_3 and C_4), a DC shifting capacitor (C_5), and a single-ended error amplifier. The overall CMFB amplifier is made up of the error amplifier and the output section of the core block, i.e. the inverter stage. Selecting $C_3 = C_4 = C_5 \equiv C$, the desired value of the common mode output voltage, $V_{DD}/2$, is obtained. As for the implementation of switched-capacitors and switches, both were realized by using the minimal dimensions allowed by the technology: a capacitance of 57 fF ($8x8\mu m^2$) and a minimum length of 0.3 μm for the switches.

Although [4], and [6] proposed active SC-based CMFB circuits, our circuit is based on an error amplifier and sampling is carried out by applying a DC offset to level shift the common mode sample. In this approach, the passive feedback factor is as high as 2/3 which improves the CMFB settling process.

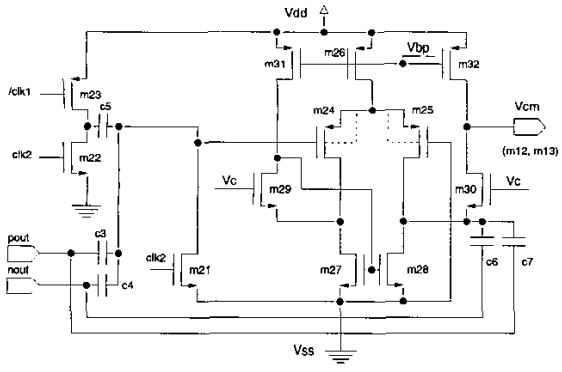

Fig. 2: Common mode feedback circuit (CMFB). The corresponding device sizes have been listed in Table 1 .

Transistor	Size (μm/μm)
m1, m2	25/1
m3	40/1
m4, m5	20/1
m6, m7	100/1
m8, m9, m10, m11	14.2/1
m12, m13	49/1
m14, m15	188/1
m24, m25	8/1
m26	12/1
m27, m28	4.8/1
m29, m30	10/1
m31, m32	6/1

Table 1: Transistor sizes. Switches were implemented using the minimum length available in this technology, i.e. 0.3 μm to limit the clock feedthrough.

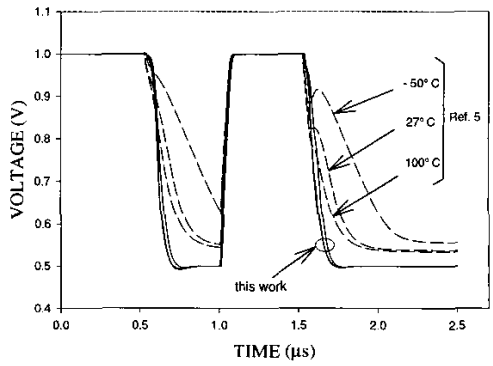

Fig. 3: Switching transients for different temperatures (Vdd = 1V). The results obtained from a CMFB circuit similar to that proposed by Reference [5] has been included for comparison.

2.2. Simulated results

Next, the complete opamp characterization was carried out. Specifically, we are going to focus our attention on the common mode opamp response. The input common mode ranges from -500 mV to +150 mV. The CMRR was higher than 120 dB and the common-mode settling time was estimated at 300 ns from a transient induced by a step of 400 mV applied to the common mode input. In consequence, it can be concluded that just one clock cycle is needed in order to precharge averaging capacitors and stabilize the common mode output.

Figures 3 and 4 show the switching transients for different temperatures and power supply voltages conditions, respectively. The capacitors size demanded for the circuit proposed in Reference [5] is higher than that of our circuit since the former directly drives the big transistors of the core output stage. On the contrary, the switched capacitors of our CMFB circuit drive the small input tran-

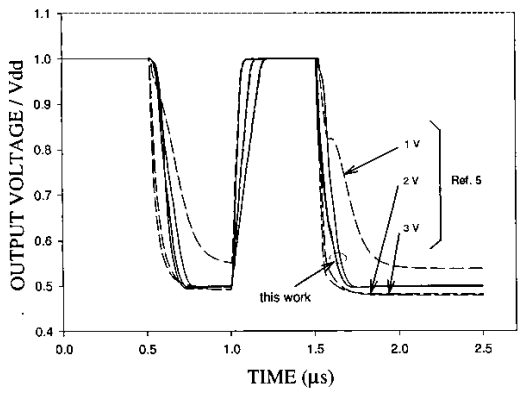

Fig. 4: Normalized switching transients for different supply voltages (T = 27°C). The results obtained from a CMFB circuit similar to that proposed by Reference [5] has been included for comparison.

Parameter	Simulated Value
Power consumption	90 μW @ 1 V
GBW	5.5 MHz
Open loop gain	85 dB
SR_{up}	4.6 V/μs
SR_{down}	5 V/μs
Switching Time	300 ns
Active area	0.016 mm^2

Table 2: Opamp performance. Simulations were carried out with a capacitance load of 5 pF.

sistors of the error amplifier that provides a virtual ground. Thus, from the silicon area point of view, our CMFB circuit gives rise to no excessive die area penalty. Moreover, while in Reference [5] the voltage gain of the CMFB amplifier is only provided by the output inverter stage, both the error amplifier and the inverter stage gains contribute to the overall CMFB voltage gain. This higher gain allows a higher accuracy to be obtained under different temperature and power voltage supply conditions.
In Table 2, the values of some important opamp parameters have been summed up.

3. SWITCHED OPAMP-BASED BANDPASS SC FILTER

3.1. Filter design

As an application of the switched opamp, a SC fully differential biquad bandpass filter for Radio Data System subcarrier detection has been designed. Thus, a nominal center frequency equal to 58 KHz was selected. The association of some similar sections gives rise to a practical RDS filter.
An E00 Fleisher-Laker topology (Figure 5) was considered due to the lower total capacitance (lower area) and spread capacitance required.

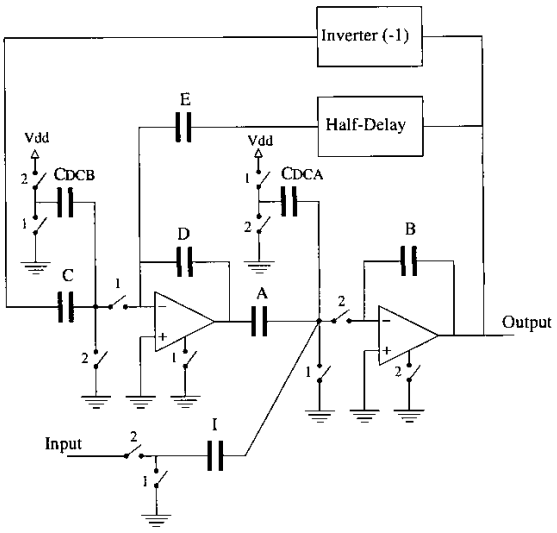

Fig. 5: Bandpass filter architecture. A single-ended topology has been shown for simplicity, while the circuit realization is fully differential.

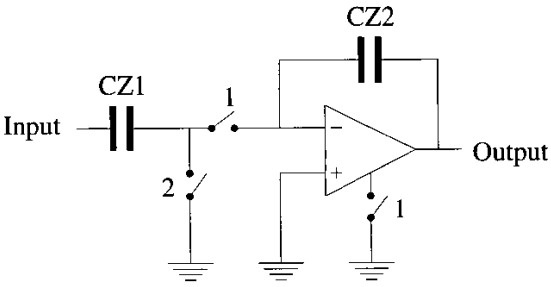

Fig. 6: Half-delay block based on a switched-capacitor amplifier.

As the filter's opamps are active in different clock phases, the E-type topology demands the inclusion of a half-delay block in the branch of the E-capacitor. This block was implemented by a switched-capacitor amplifier with unity gain, deploying the switched opamp technique (Figure 6) [3], [6]. If the capacitors are selected $C_{z1} = C_{z2}$, then $V_{out} = V_{in}$.
For a clock frequency of 1 MHz, the capacitor sizes for the filter referred to an unit capacitance, C_u, of 225 fF (16x16μm^2) are the following: C_A = 1.91, C_B = 5.24, C_C = 5.41, C_D = 15.18, C_E = 1.00, C_I = 1.00, C_{DCA} = 0.96, C_{DCB} = 2.71, and $C_{z1} = C_{z2}$ = 1.00.

3.2. Simulated results of the filter

All the simulations were obtained by using a power supply voltage of 1 V, and the power consumption is 230 μW. The basic filter parameters were obtained from the frequency response (Bode plot, Figure 7): f_0 = 57986 Hz; quality factor, Q = 15.5; and, finally, voltage gain, A_V = 8.3.

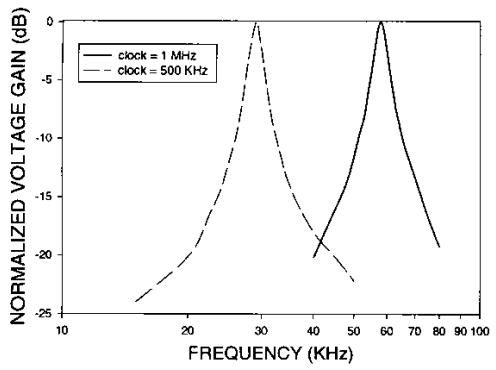

Fig. 7: Filter frequency response: Bode plot for two different clock frequencies.

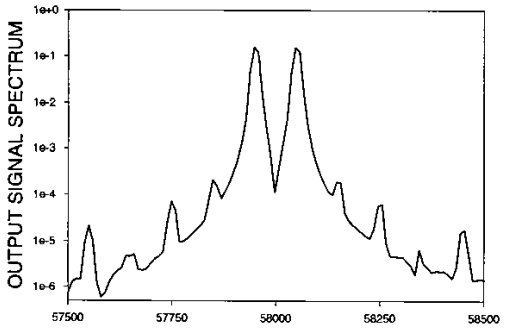

Fig. 8: Output intermodulation spectrum for two input single-tones of 57950 and 58050 Hz (resolution: 10 Hz).

As a quantitative estimation of the validity of the differential approach to provide immunity with respect to noise on the supply, the Power Supply Rejection Ratio (PSRR) in the bandpass and the Power Supply Rejection (PSR) up to f_s have been measured. Both were better than -40 dB.
Nonlinearity in a balanced circuit is mainly measured by third-harmonic distortion, and in the case of a bandpass circuit, by the third-order intermodulation created by two inband tones. When two input signals are applied, the measured input IP3 (IIP3) is 6 dBm (1.3 Vpp). This value is higher than power supply voltage. In Figure 8, the output spectrum corresponding to two 20 mV amplitude input signals has been included. As can be seen, the intermodulation components are at -60 dBc. These results suggest a high filter linearity.
An important filter parameter, such as the Dynamic Range, will be obtained when the experimental noise floor is measured. Currently filter prototype fabrication is in progress and experimental results will be shown at the Conference.

Parameter	Simulated Value
Technology	0.35μm CMOS
Supply voltage	1 V
Power consumption	230 μW @ 1 V
Sampling frequency	1 MHz
Central frequency	57986 Hz
Quality factor	15.5
Voltage gain	8.3
PSSR, PSR	-40 dB, -40 dB
IIP3	6 dBm
Active filter chip area	0.13 mm^2

Table 3: Filter performance.

4. CONCLUSIONS

In this paper, a fully differential SC bandpass filter based on the switched opamp approach has been designed and realized in a 0.35 μm CMOS technology which operates at 1V and is clocked at 1 MHz. Table 3 sums up the filter performance.
As an internal filter component, a fully differential switched opamp has also designed with a switched-capacitor common mode feedback that only operates on the output stage. This CMFB circuit is based on an error amplifier and provides an accurate common-mode output for a wide temperature and supply voltage ranges. Both the opamp and the filter were simulated with the Spectre program by using the extracted circuit from the layout.

5. REFERENCES

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